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SIGNAL PROCESSOR FOR UNATTENDED RADAR (SPUR) PHASE II.(U)

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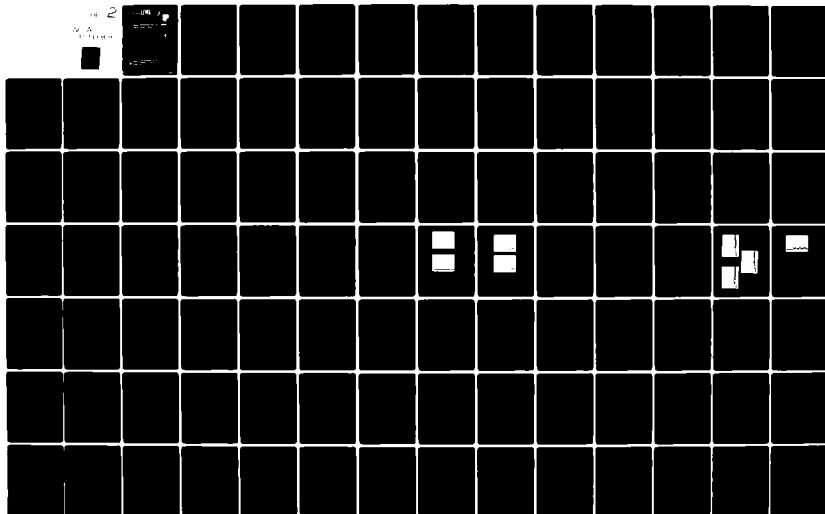
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SIGNAL PROCESSOR FOR UNATTENDED RADAR (SPUR) PHASE II

ITT Gilfillan, Inc.

John M. Milan
Charles D. Lucas, Jr.
Daniel M. Kikuta

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ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, New York 13441

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APPROVED:

Ernest J. Timpin
ERNEST J. TIMPIN
Project Engineer

APPROVED:

Frank J. Keen
FRANK J. KEEN
Technical Director
Surveillance Division

FOR THE COMMANDER:

John P. Huss
JOHN P. HUSS
Acting Chief, Plans Office

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21. ABSTRACT (Continue on reverse side if necessary and identify by block number) This final report documents the results of a five-month Validation Program conducted during Phase II of a contract to examine Signal Processing for Unattended Radars. The Validation Program was based on risk reduction recommendations generated during Phase I of the SPUR: Conceptual Design. Identified critical circuits and firmware were designed, some developed, and some tested to validate the estimates of reliability, power, functional performance, fault monitoring and			

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recovery, and stability of the recommended processor. Recommendation for further development and testing are included.

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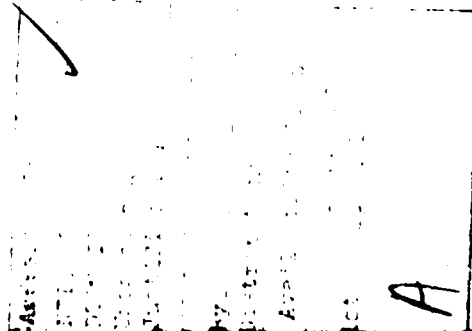
EVALUATION

The objective of the SEEK FROST program was to re-equip the DEW line with modern sensors. The requirements were stated in ADCOM ROC 5-75. A study was undertaken by MITRE to examine various system alternatives for satisfying the requirements (Northern Air Surveillance Study). This study concluded that the optimum approach consisted of a chain of unattended, short-range radars. Further analyses lead to the final system configuration consisting of 13 long range radars which would be augmented for low level coverage by 57 unattended gapfillers.

In 1976, RADC awarded three (3) ESD sponsored parallel study contracts to examine the technical and economical feasibility of an unattended radar. These studies concluded that radars with unattended operation exceeding three (3) months were feasible and economical.

As a result of issues which surfaced during the evaluation of the Unattended Radar Studies, a series of validation efforts commenced during the FY 78 - FY 79 time. The effort reported here was a part of the SEEK FROST validation program - The intent being to look at issues of (a) reliability, (b) self-monitoring, calibration and reconfiguration, (c) power demand - all critical aspects of unattended operation.

SPUR was conceived originally as a two (2) phase program. Phase I examined the technology available to support signal processing and provided a conceptual design for hardware realization. That effort is reported in RADC-TR-79-243, "Signal Processor for Unattended Radar", dated October 1979. The intent of Phase II was to provide hardware verification of concepts developed in Phase I. Phase II had just begun when funding for the SEEK FROST program was deleted by Congress forcing a truncation of the effort. However, some critical aspects were verified and clear avenues for future productive development emerged.



The project was sponsored jointly by RADC (PE 62702F, Project 4506) and ESD (PE 12412F, Project 2488) and supported TPO RIC.

Eugene J. Tippie
EUGENE J. TIPPIE
Project Engineer

FOREWORD

This Final Report documents the activities conducted during the five-month Phase II Validation Program of the Signal Processor for Unattended Radar (SPUR), Contract No. F30602-78-C-0288. Included in this report is a summary of the optimum SPUR (recommended as a result of SPUR Phase I, Conceptual Design), the complete recommended Validation Program, and the results of the Validation Program.

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Section 1

INTRODUCTION

The Signal Processor for Unattended Radar (SPUR) Phase II Validation Program was a verification effort for the SPUR Phase I Conceptual Design. During the Conceptual Design, the optimum processor for an unattended radar was configured and its parameters estimated¹. The Validation Program was designed to validate these results for critical circuits of the processor.

These programs were a continuation of the U.S. Air Force efforts to utilize advancing technology to counter the ever-increasing manpower costs in operating and maintaining defense equipment. These efforts have focused on unattended radar concepts and during the 1976 UAR/MAR Radar Design Studies, by ITT Gilfillan, General Electric, and Raytheon, one of the major conclusions of the studies was that the signal processor is the critical element of the system. This conclusion is particularly true in terms of reliability and prime power requirements. Consequently, the SPUR Program was funded with the objective of defining and validating an optimum processor design.

The SPUR Phase I Conceptual Design is summarized in Section 2. This summary includes the definition of the requirements, optimization criteria, and recommended design. The Validation Program, recommended as a result of Phase I, is discussed in Section 3. This twelve-month program selected critical circuits for validation of power, reliability, functional performance, fault monitoring and recovery, and stability.

The results of the actual SPUR Phase I Validation Program are presented in Section 4. The actual program had a schedule reduction to five months with a commensurate reduction in verification tasks. This reduction resulted in considerably reduced hardware testing from the original plan. However, several detailed designs were completed to the point that power and reliability calculations could be made which were representative of the expected final values for the circuits.

The recommendations as a result of the Phase II Program are presented in Section 5.

Five Appendices present supporting data including the Preliminary Phase II Test Plan and four design-related documents. The documents present the requirements for detailed design of four functions judged critical to the performance of the optimum SPUR.

¹ Milan, John M., et al, Signal Processing for Unattended Radar, Final Technical Report, RADC-TR-79-243, October 1979.

Section 2

SPUR CONCEPTUAL DESIGN SUMMARY

The SPUR Phase I Conceptual Design configured an optimum processor, and important parameters of that processor. The results of this effort are summarized in the next three sections.

2.1 SPUR PERFORMANCE GOALS AND PARAMETERS

The SPUR Conceptual Design Phase optimized a bounded processor for an unattended radar, subject to a set of performance, functional, and environmental goals. The bounded processor was defined as performing those functions occurring between the video phase detectors and the declaration of a target following postdetection integration. Hence, the optimization considered those functions normally termed *signal* processing as opposed to *data* processing.

The initial parameters for the SPUR design were of two types – 1) major performance and functional parameters used as guidelines for the processor conceptual design, and 2) models defining the expected clutter environment. A third group of parameters defining a baseline radar system was later used for performing the analyses and tradeoffs.

The major parameters (Table 2-I) for the SPUR served to bound the optimization of the signal processor to a reasonable set of alternatives. In order to provide maximum applicability, these goals were selected such that the optimum SPUR was as independent of other radar parameters as possible.

The clutter environment models (Table 2-II) were specified for land, sea, and weather clutter. During the optimization it was assumed that more than one type of clutter (i.e., land and weather) might be present at the same time in a particular range cell. Second time around clutter was also considered during the analyses.

While the SPUR requirements discussed above depend very little on basic radar parameters, additional radar-specific assumptions were required in performing detailed analyses and tradeoffs. These parameters (Table 2-III) were used in clutter, signal-to-noise ratio (S/N), and loss calculations, for example. In general, these parameters affected the implementation requirements (i.e., resolution in A/D converters, memory and processor dynamic range), but they did not strongly impact the basic architecture of the processor.

2.2 OPTIMIZATION CRITERION

Configuring a signal processor for most radars is often relatively unconstrained; i.e., the only explicit constraint is the set of performance requirements tempered by the implicit constraint of acquisition cost. The signal processor is therefore designed to achieve an acceptable level of performance at a minimum cost.

*Table 2-1. Requirements and Parameters Established
to Bound the Spur Study Effort*

Performance:

Range	5-60 nmi
Range Resolution	0.1 nmi
Land Clutter Improvement Factor	> 50 dB
MTBF	20K to 100K hrs

Functions:

Pulse Compression	32:1
Spectral Filtering	8-Pulse
CFAR	32 Cell Averaging
Clutter Map	Zero Velocity Superclutter/ Intraclutter Detection Processing
MTI	In Conjunction w/Spectral Filtering
Postdetection Integration	4 Pulses

Environmental:

Operating Temperature Range = 0°F to +120°F
Storage Temperature Range = -70°F to +100°F

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For the SPUR Phase I Conceptual Design, a processor optimized to operate unattended in a harsh environment was the goal. The unattended nature of the application leads to additional explicit constraints on the processor design, while the requirements for optimality necessitates an evaluation system or method for selection of the best approach (i.e., on optimization criterion).

For the SPUR, six constraints were accepted explicitly. These constraints were performance, reliability, cost, maintainability, risk, and power. The constraints on reliability, maintainability, and power become explicit constraints because of the unattended nature of the processor. Reliability includes evaluation of automatic calibration and repair capabilities (i.e., use of selective redundancies) as well as calculation of MTBF. Maintainability includes use of modular packaging, BITE, and remove and replace repair. Risk evaluation is based on projecting the present technology and known processing methods to the preferred embodiments.

Table 2-II. A Clutter Model that Characterizes the Spur Radar Environment

Land Clutter		
Amplitude Distribution	Log — Normal	
Reflectivity		
Median	-34 dB m ² /m ²	
84th Percentile	-24 dB m ² /m ²	
Spectrum (Gaussian)		
Standard Deviation (30 knot wind)	0.2 m/sec	
Sea Clutter (Sea State 4)		
Amplitude Distribution	Rayleigh	
Reflectivity/Grazing Angle/ Polarization	H	V
1.0 degree	-52	-45 dB m ² /m ²
3	-48	-38
10	-45	-31
Spectrum (Gaussian)		
Mean Velocity	2.5	1.3 m/sec
Standard Deviation	0.9	0.9 m/sec
Weather Clutter (15 mm/hr Rain)		
Cell Diameter	5 nmi	
Ceiling	30K ft	
Radial Velocity	0 to 80 knots	
Shear	0 to 80 knots from 0 to 50K feet with any arbitrary shear distribution over this altitude range	
Amplitude Distribution	Rayleigh	
Reflectivity	-88 dB m ² /m ³	

Table 2-III. Additional Radar Parameters Assumed in Conducting Performance Tradeoffs and Analyses

Baseline Radar Parameters:	
Antenna Beamwidths	
Azimuth	3°
Elevation	30°
Antenna Rotation Rate	15 rpm
Target Velocity	±2400 Knots
Probability of Detection	90% (after PDI)
Probability of False Alarm	2 x 10 ⁻⁵ (after PDI)

In order to define an optimal SPUR design, a weighting matrix of the above constraints was developed. The weighting matrix (Table 2-IV) was used in quantitatively evaluating alternative functional algorithms, architectures, and implementations. The particular weights were selected to indicate the relative importance of each constraint on the optimum design.

Table 2-IV. The Optimization Criterion uses a Weighted Combination of Six Constraints

	<u>Weighting</u>	<u>Comments</u>
Reliability *	10	Fault-Tolerant Design *
Performance	10	Meet Requirements
Cost	7	60 Systems
Maintainability *	6	Remove and Replace Concept
Risk	6	Near Term Requirement Reduces Risk
Power	5	Minimize

* Fault-tolerant design improves maintainability.

In using the weighting matrix technique, data from each category was normalized to the most desirable alternative and multiplied by the weighting factor before final summation. Thus, the lowest score achieved in the comparisons corresponds to the recommended alternative.

By using the weighting matrix of explicit constraints as the optimization criterion, the optimal SPUR was developed through a set of tradeoffs. This optimal SPUR is reviewed in the next Section.

2.3 OPTIMUM PROCESSOR

During SPUR Phase I Conceptual Design, the optimum processor was defined using the optimization criterion developed in the previous section. This processor, and the tradeoffs performed to arrive at the recommended configuration, are described in detail in the SPUR Phase I Final Report.¹ However, a brief summary of the optimum SPUR is generated in this section.

The recommended optimum SPUR is a unified solution providing the required signal processing for a modern, 2D, medium range, unattended radar, operating in severe clutter in a harsh environment. The specifications for the optimum SPUR illustrate that the basic SPUR goals (see Section 2.1) have been met or exceeded in most cases by the recommended design (Table 2-V). Some special features of the processor are listed in Table 2-VI.

The block diagram of the SPUR (Figure 2-1) illustrates the five generic functions defined at the beginning of the conceptual design and the processing performed in each function.

The five functions are:

- 1) Analog and A/D Processing Function,
- 2) Doppler Processing Function,
- 3) Zero Channel Processing Function,
- 4) Post-Detection Processing Function, and
- 5) STATE (Status, Transformation, and Test Evaluation) Processor Function.

The Analog and A/D Processing Function consists of three A/D converter units (two active and one spare) with fault detection (BITE), isolation, and replacement switching located on one 14 x 15 inch board. Thus the A/D converter is a self-contained unit from a reliability viewpoint; hence, it reports only its status to the STATE Processor. The A/D's provide 11 bit resolution at a 1.62 MHz sampling rate for both I and Q video. Each A/D is stabilized against zero drift by a calibration loop which monitors the most significant bit (MSB) and feeds back a correction signal to the associated video amplifier for that channel. The noise level relative to the least significant bit (LSB) is stabilized by a loop monitoring the I and Q outputs of the active converters and which feeds back a correction signal to the gain control of the IF amplifier in the receiver.

A tradeoff analysis between a single board design for the A/D Converter System and a multiple board design with only one A/D Converter per board was performed. As discussed below, the result of that analysis was the recommendation of the single board A/D Converter System design described above.

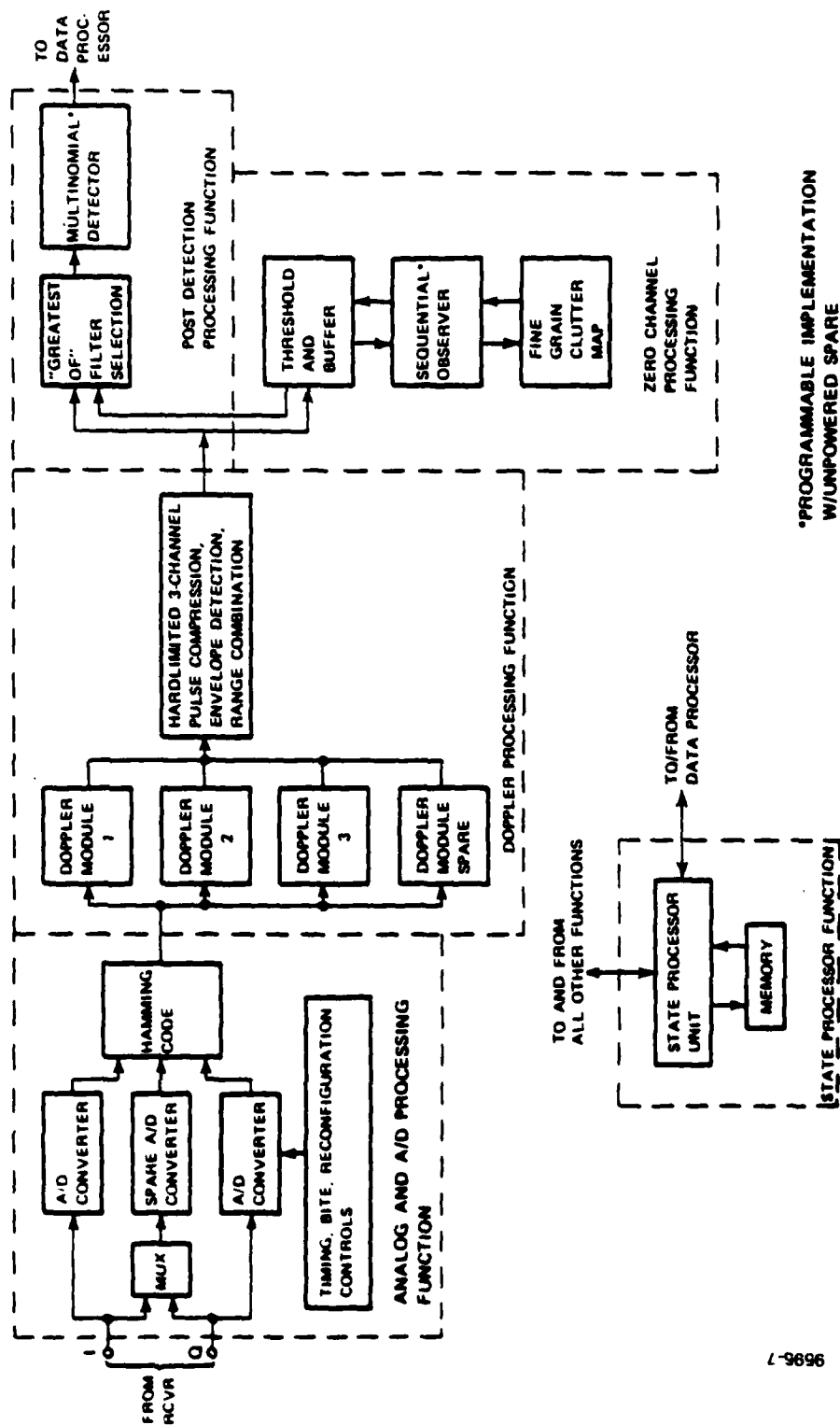
¹ Milan, John M., et al, Signal Processing for Unattended Radar, Final Technical Report, RADCR-79-243, October 1979.

**Table 2-V. Overall Specifications for the Spur Define
an Advanced Highly Reliable Signal Processor**

<u>Specification</u>	<u>Goal</u>	<u>SPUR</u>
Range	5-60 nmi	5-60 nmi
Range Resolution	0.1 nmi	0.1 nmi
Land Clutter Improvement Factor	>50 dB	50.9
Pulse Compression Ratio	32:1	31:1
FFT	8-Pulse Optimum Weights	Narrowband Near-Optimum
MTI	3 Pulses	Filter Bank operating on 9 Pulses
Range Average CFAR	32 Sample	31-bit hard limited pulse compression
Clutter Map	Zero Velocity Superclutter/ Intraclutter Detection Processing	Zero Velocity Intraclutter Detection Processing
Postdetection Integration	4 Samples	4 Samples
prf's	2 Available	4 Recommended
MTBF	20,000 to 100,000 hours	22,331 hours
Power	Minimize	226W
Processing Gain	—	0.15 dB Worst Case
Maintainability	For unattended operation in remote, harsh environments	Remove and replace concepts

**Table 2-VI. Some Prime Features Incorporated in the Optimum
Processor Design**

Double Sampling in Range
 11 Bits A/D Conversion
 Near Optimum Filter Doppler Processing (9 pulses — 6 filters)
 31-Bit Binary Phased-Coded Pulse Compression with offset
 channels for high velocity targets
 Hard-Limited CFAR
 Zero Doppler Processing for Intraclutter Visibility of Crossing
 Targets
 Multinomial Post-Detection Integration (4 pulses)
 Distributed BITE with STATE Monitor and Controller



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Figure 2-1. Overall block diagram of the SPUR which defines the five selected processing functions and operations performed in each.

The major advantages of each design are

Multiple Board Design Advantages -

- a) the repair of a single failed converter can be accomplished with the radar in operation, and
- b) the sparing of boards containing single A/D converters is less expensive than sparing boards containing the A/D Converter System.

Single Board Design Advantages -

- a) simplification of fault-detection, isolation, and automatic repair process,
- b) simplification of the design and placement of the recommended automatic calibration circuitry,
- c) selection of a single common board size for each of the SPUR modules, and
- d) minimization of the card cage design.

The replacement of a single failed converter while the radar is in operation is recognized as an advantage of the multiple board design. This advantage is particularly clear in past designs in which the converters had relatively high failure rates and troubleshooting was required to isolate a failure. However, in the SPUR, with its emphasis on the remove and replace maintenance concept and unattended operation, this advantage has been reduced. The remove and replace concept, along with the fault-detection and isolation recommended for the SPUR, ensures that maintenance action to repair a single board design can be performed with minimal disruption of operation; i.e., less than five minutes based on maintainability demonstrations using similar boards. Coupled with the minimal disruption is the low probability (based on the technology gains of LSI) of requiring this maintenance action: 12 percent at a three-month interval and 41 percent at one year (calculated using the serial failure rate of the converters). A key design feature which aids the single board design (and which must be triplicated for the multiple board design) is manual control of the board power. Then, during the maintenance action, only power to the A/D Converter System is interrupted. Dynamically stored data (e.g., clutter map data) in the system is not affected. The STATE Processor notifies the system when the A/D Converter is removed and when normal operation is restored.

The unattended nature of the SPUR further affects maintainability. Some repairs will not be performed until two A/D converters have failed. In this case, the radar will be taken off of the air with either design. However, while maintenance actions of this type are possible, they will be rare; e.g., probability of two converter failures by three months is two percent, and this probability at one year (with no maintenance) is eight percent.

The cost advantage of the multiple board design with single spare approaches 1.5:1 in a conventional radar system when the cost of three boards is equal to the cost of the one board in the single board design. However, in the SPUR, this cost advantage reduces to on the order of 1.25:1 for the converter sections because of the repartitioning necessary in the

monitor and self-repair circuitry which necessitates triplication of some hardware. In addition, as described below, the multiple board design will require not only the three converter boards but also an additional board to hold circuitry needed for automatic calibration. When the spares requirements are included in the above costs, the apparent cost advantage of the multiple board design is further reduced.

The advantages of the single board design are generally related to the increased reliability and maintainability requirements of the SPUR. The fault-detection, isolation, and self-repair circuitry is simplified because in the single board design this self-repair related hardware is placed directly on the board. In a multiple board design, most of this circuitry is triplicated with error decisions made by the STATE Processor, or resides on a separate board interfaced to the three A/D Converters and the STATE Processor. This latter design increases the multiple board requirement to four smaller boards to replace the one large board (14 inches x 15 inches) in the single board design.

Similarly, the gain control calibration loop resides on the board in the single board design. In the multiple board design, this circuitry must reside on a separate board because it operates on the two active channels of the A/D Converter System. This placement requires interfacing of the loop to the STATE Processor for selection of active channels.

The third advantage of the single board design is a maintenance and handling advantage. Selection of a common board size for each of the SPUR modules results in standardized shipping containers for transportation and standardized maintenance handling procedures and cautions. A simple keying system for the boards prevents improper installation. In the multiple board design, two sizes of boards are used in the system, which necessitates doubling the maintenance equipment required for support of the SPUR.

In using a single board design, the card cage for SPUR is simplified, because a single cage handling a minimized number of common size boards utilizing a single backplane is required. With the multiple board design, the packaging is expanded and the interconnections are increased.

The Doppler Processing Function consists of two units: 1) Doppler Modules, and 2) Post-Filtering Processor. The Doppler Modules implement the recommended Near Optimum Filterbank consisting of six filters including the zero filter. These six filters operate on eight of the nine pulses in a coherent group (the first pulse is a fill pulse). Each filter is generated by eight complex multiplies and seven complex additions. The MSBs of this set of operations (hardlimited data) are sent to the Post-Filtering Processor. Sixteen bits of the computational result are available to the STATE Processor for BITE operations. Four separate boards (including one unpowered spare) are recommended for the SPUR and hence the STATE Processor performs BITE evaluation and recovery operations for this function.

The Post-Filtering Processor (PFP) unit receives the hardlimited data from the Doppler Modules in range bin order and performs 31-bit hardlimited pulse compression on it. Because binary phase-coded pulse compression is relatively Doppler sensitive, a special implementation for the pulse compression is recommended.² The pulse compression is performed in the equivalent of three channels (for zero, positive, and negative target Dopplers) by splitting the code into two sections, of 15 and 16 bits. The appropriate antiphase rotations are performed and the sections are recombined. Each equivalent channel is detected, $(\max \{I, Q\} + 1/4 \min \{I, Q\})$, and the channel with the maximum response is selected by a "greatest-of" circuit for further processing. The data is reduced to a single sample per range bin by adding adjacent odd and even samples (i.e., $R_i + R_{i+1}$, i odd). It is sent to the Zero Channel Processing Function when the data is from the zero filter, and to the Post-Detection Processing Function when the data is from any of the remaining five filters.

The PFP is located on one 14 x 15 inch board. It is monitored by the STATE Processor for reliability evaluation but contains no reconfigurable functions since its failure rate is relatively low.

The Zero Channel Processor performs control on the zero filter such that, when ground clutter is present, its output is censored from the Post-Detection Processor. The Zero Channel Processor consists of a censor process and a fine grain clutter map. The censor process, using a sequential observer technique (a form of scan-to-scan averaging), determines when ground clutter is present in a particular clutter map cell. The fine grain map stores this data for all map cells in the coverage area of the radar. The recommended clutter map cell size is $3/4^\circ \times 0.4$ nmi (i.e., one coherent group by four range bins); therefore, 2^{16} map locations are provided. The Zero Channel Processor has the censor process implemented in a programmable processor, the RPM-II. The clutter map, program memory, and interface to the RPM-II are located on an interface board. The STATE Processor controls the BITE operations of the interface board, the extended BITE requirements for the RPM-II, and test evaluation. A spare unpowered RPM-II is provided for redundancy and the STATE processor controls this reconfiguration.

The Post-Detection Processor (PDP) receives six-bit data from the PFP from all filters except the zero filter (which comes via the Zero Channel Processor Function). The PDP performs the "greatest-of" function across the five or six filters and performs multinomial integration over one azimuth beamwidth (4 hits). The "greatest-of" function and the first thresholds of the multinomial detector are performed by hardware located on the same interface board as the Zero Channel Processor. The remainder of the multinomial process is performed in the RPM-II. Output results (i.e., threshold crossings) are stored in a shift register on the interface board for access by the data processor. The STATE Processor handles BITE and reconfiguration for this unit as well.

² This method of pulse compression will be the subject of a U.S. Patent Application (Ref. A-1784)

The Status, Transformation, and Test Evaluation (STATE) Processor is the unique feature of the recommended Signal Processor for the Unattended Radar. It provides a centralized focus on reliability for overall processor configuration and control. This selection assures cohesive operation and reporting for the SPUR because the STATE Processor conveys the total status of the signal processor to the data processor and beyond. It performs the monitoring of all units of the SPUR and the reconfiguration control on all but the A/D converter system which has its own capability for reconfiguration control.

Since the STATE Processor is at the heart of the SPUR, it is extremely important that it be a highly-reliable unit. The recommended basic unit for the STATE Processor is the MC68000 microprocessor in a Triple Modular Redundant (TMR) configuration. That is, three processors perform the same task and the results are voted upon to form the final output. A hardware power-on and external reset capability is also provided.

The STATE Processor having these features fits on one 14 x 15 inch board and consumes approximately 22 watts. The recommended storage is 16K of program memory and 2K of data memory.

Section 3

PHASE II VALIDATION PROGRAM

The prime objective of the SPUR Phase II Validation Program is to verify selected parameters and characteristics of the optimum SPUR conceptual design. The recommended program was based on the desire to reduce risk in the optimum solution by designing, fabricating, and testing circuits identified as critical to the expected operation of the conceptual design. The twelve-month program, initially developed during the Phase I effort and revised early in Phase II, is described below. The results described in Section 4, Validation Results, are based on the reduced five-month schedules. Changes in the program are discussed there.

In order to maximize the expected benefits of the verification effort subject to the fixed cost constraints of the contract, maximum usage of existing or modifiable equipment was recommended. Consequently, in some cases, the validation of a function used a non-preferred implementation method (from the viewpoint of power, reliability, or cost, for example) to demonstrate another parameter, such as functional performance. The validations of the remaining, non-demonstrated parameters for that function were accomplished by analysis and computation using generally accepted models.

Identified risks in the SPUR conceptual design fell into two categories: processor level risks and functional level risks. The major processor risk is associated with reliability: automatic fault detection for all functions and automatic fault isolation and recovery for the selected functions with redundancy. This risk has been addressed in the optimum SPUR by utilizing a distributed BITE approach with a centralized focus for control and monitoring of processor status, i.e., defining the STATE Processor for the optimum SPUR. The Validation Program to reduce this risk is to demonstrate fault detection through BITE on each module fabricated for SPUR, and to demonstrate an example of fault isolation and recovery by using the STATE Processor interfaced with the Doppler Filter Modules. As noted below, both of these units were recommended for design, fabrication and test. Demonstrating fault-tolerance adds the requirement of integrating them together for the specific tests.

During the Phase II Validation Program, the results were continuously reviewed relative to the Phase I Conceptual Design projections. This monitoring (noting changes from the designated optimum SPUR recommendations) had particular emphasis on power, reliability and performance results.

Functional level risks (Table 3-I) were identified relative to five areas of major emphasis:

- 1) functional performance
- 2) power consumption
- 3) reliability
- 4) performance monitoring/fault isolation
- 5) stability

The following sections discuss these areas relative to validation of each function.

Table 3-1. Major Functional Level Risks and Risk Reduction Approaches

The major functional risks have been determined and plans developed for reducing these risks

<u>Function or Unit Level Risks*</u>	<u>Risk Reduction Approach</u>
<u>Analog and A/D Processing Function</u>	
Automatic Testing and Calibration of Processor Analog Circuitry	Early Conversion to Digital Domain Calibration Feedback Loops. Design, Develop, Test Example of Calibration Loop
Parameters of A/D Converter	Detailed Design of Two-step Flash Converter
<u>Doppler Processing Function</u>	
Doppler Filter Modules Achievable Improvement Factor Filter Losses	Develop two Doppler Filter Modules Test Partial Filterbank against Severe Clutter Test Filter Shape
Post-Filtering Processor Pulse Compression and CFAR Losses	Modify Existing Pulse Compressor Test Pulse Compressor in L-band System
<u>Zero Channel Processing Function</u>	
Cell Size Realtime Operation	Test Modified Clutter Map System Against Severe Clutter Measure CPU Utilization for Sector
<u>Post-Detection Processing Function</u>	
Realtime Operation	Develop PDP Firmware Test in RPM-II (CPU Utilization)
<u>STATE Processor</u>	
Internal Reliability Monitor and Control Other Processor Functions	Develop STATE Processor Test Firmware Demonstrate with DFM's

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*Reliability and Intraunit Reconfigurations are potential risks to all units.

3.1 ANALOG AND A/D PROCESSING FUNCTION

The Validation Program for the A/D converter system, the principle element of the Analog and A/D Processing Function, addresses the reduction of two types of risk. The first risk type, automatic testing and calibration of analog circuitry (i.e., analog stability), exists nowhere else in the SPUR processor and hence is of special importance. This risk has been minimized in the optimum SPUR by converting to the digital domain as early as possible and by specifying calibration loops for both zero drift and gain fluctuations. The second risk type is the achievement of the parameters of the optimum SPUR design for an 11 bit, relatively fast, converter at a reasonable cost. The recommended implementation, based on a preliminary design, was estimated to perform to the requirements.

Verification of the entire A/D system is not possible due to cost constraints. However, the above two types of risk were to be substantially reduced by the following verification program:

- a) Design and develop example of automatic calibration circuitry,
- b) Test calibration circuitry with existing A/D converter,
- c) Conduct preliminary design of two-step flash A/D converter unit, and
- d) Verify conceptual design based on combination of preliminary design and developed hardware.

The particular automatic calibration circuit recommended for development was the zero drift loop. Analog stability was scheduled to be demonstrated by testing this loop using an existing 10 bit (9 bits + sign) A/D converter operating at a sampling rate of 5.18 MHz. The loop monitors the MSB's at the I and Q channels and feeds correction signals back to the respective video amplifiers of the two channels.

Power consumption was estimated based on the developed calibration loop and interface circuitry and the detailed design. Reliability was similarly estimated.

3.2 DOPPLER PROCESSING FUNCTION

The Validation Program for the Doppler Processing Function addresses reduction of risk associated with two units: the Doppler Filter Modules (DFM) and the Post-Filtering Processor (PFP). These risks and verification recommendations are discussed separately below for the two units.

The major unit level risks for the DFM are associated with functional performance; particularly, achievement of the required MTI Improvement Factor, operation against bimodal and second-time-around clutter, and minimization of processing losses. These risks were reduced in the optimum SPUR by specifying a Near Optimum Filterbank, providing individual CFAR on each filter, and adding a fill pulse to the coherent group.

The Validation Program to verify this risk reduction was to:

- a) design, fabricate, and test two DFM's
- b) integrate the DFMs into an L-band demonstration radar and test against clutter
- c) Integrate the DFMs with the STATE Processor and test fault recovery operations.

Fabrication of two of the four DFM's required for a full SPUR was recommended to minimize cost in the validation. Developing two boards provides a partial filter bank (four of six filters) which, when integrated into the radar, allows evaluation against severe clutter in functional performance tests. Having two boards also allows demonstration of performance monitoring and fault isolation/recovery techniques when integrated with the STATE Processor. Faults are simulated in the DFM's and evaluated by the STATE Processor response to the BITE results. These faults include failures in the circuitry common to the two filters per board such that two filters are disabled simultaneously.

Additional unit tests were to be made at the board level. Filter shape and S/N loss are examples of functional tests which may be performed on a single board. Power consumption was to have been measured on each board and extrapolated for the full system under the two conditions of operation: three boards active and one in unpowered standby, and four boards powered but two channels unused. Reliability was estimated by computation according to MIL-Hdbk-217C using the actual detailed design components and appropriate accounting for the redundancy in the design. The stability of the circuitry is assured after debugging because of the digital nature of the design and the selection of components which are specified over the expected environmental conditions.

The major unit level risks of the PFP also are associated with functional performance; namely S/N losses and sidelobes associated with substantial Doppler velocities on targets when using binary phase-coded pulse compression. The reduction method in the optimum SPUR was the recommendation of the novel pulse compression system providing the equivalent of three channels.

The validation program to verify this risk reduction was to:

- a) modify an existing single channel pulse compressor by adding the two additional channels.
- b) integrate the resulting PFP into the L-band radar and test.

Modification of an existing pulse compressor was recommended to save cost. Validation of the functional performance of the unit in the radar was recommended because it bypasses the building of a rather elaborate test fixture for measuring probability of detection vs. S/N at a given probability of false alarm. Performance is also evaluated in a severe clutter environment which is important to assess the effects of increased sidelobes in the unit.

Additional unit tests were performed at the board level. These tests verify functional operation and performance monitoring/fault isolation by the use of on-board BITE. Power consumption was verified by measuring the power consumed by the modified section (on a separate board from the original pulse compressor) and extrapolating to the full power for the function. This method was required because the existing pulse compression board does not implement the pulse compression in the preferred method. Reliability was computed in a similar manner by calculating the reliability of the modifications according to the detailed design and extrapolating to the full function reliability. Stability is assured by the digital design.

3.3 ZERO CHANNEL PROCESSING FUNCTION

The Validation Program for the Zero Channel Processing Function addresses the reduction of functional performance risk and implementation risk. The risk associated with functional performance is related to cell size in the fine grain clutter map, while implementation risk is the ability of the processor to update the cell information in realtime such that this process and the Post-Detection Processing (PDP) Function can both be accomplished in one microcomputer, the RPM-II, as recommended by the optimum SPUR design.

The Validation Program was to:

- a) modify a general clutter mapping system, being separately developed, such that SPUR clutter map cell sizes can be evaluated, and
- b) test this system in an L-Band radar using a zero channel filter developed from an FFT filter bank (8 point).

This verification method was to limit evaluation of the mapping operation to an area sector of approximately 30 nmi by $22\frac{1}{2}^{\circ}$ which can be located as desired relative to a north pulse. The reduced area coverage is due to memory constraints. The implementation in the RPM-II will be evaluated by measuring CPU utilization. The functional performance was to be evaluated by operation against severe clutter which is placed at designated points relative to the mapped area. Edge effects are particularly important and were to have formed a major part of the evaluation. A key parameter of a clutter map with small cells, the stability of the map, was also to be evaluated.

3.4 POST-DETECTION PROCESSING FUNCTIONS

The Validation Program for the PDP Function, implementing a multinomial detector, addresses the implementation risk as defined previously for the ZCP Function; i.e., accomplishing the process in realtime such that both functions can be performed in one RPM-II. The determination of the PDP Function time is more difficult to validate, however, because it is data dependent; i.e., it depends on the number of crossings of the first set of thresholds. The number of these crossings is dominated by crossings due to noise for the SPUR system as presently configured.

The Validation Program for the Post-Detection Processing Function was to:

- a) develop the firmware program for the PDP function, and
- b) evaluate the firmware program running in an RPM-II.

The verification was to have validated the operation of the PDP firmware and allowed a measure of the time required for the processing (measured by CPU utilization) as a function of noise loading.

The results here would have been combined with the ZCP results for validation of running both programs simultaneously in one processor.

3.5 STATE PROCESSOR

The Validation Program for the STATE Processor, the centralized focus for reliability for the optimum SPUR, assesses the risks inherent in providing internal redundancy to meet stringent reliability requirements of the unit and in providing flexibility for monitoring and controlling the other functional areas relative to reliability.

The Validation Program was to:

- a) design, fabricate, and test the STATE Processor hardware,
- b) develop internal verification firmware,
- c) develop integration firmware for the DFM's, and
- d) integrate the STATE Processor with the DFM's to demonstrate the fault detection and recovery using redundant modules.

The functional performance requirements of the STATE Processor were to have been validated by demonstrating fault detection and recovery in conjunction with the DFM's after integration. Power consumption was to be measured and reliability was calculated using the standard MIL-Hdbk-217C methods with the detailed design. Performance monitoring/fault detection was to be validated using the internal verification firmware in addition to operation with the DFM's. The stability of the processor was assured by providing a reset to each processor at the start of each coherent group; these resets insure that the processors remain synchronized.

Section 4

VALIDATION RESULTS

The SPUR Phase II Validation Program, developed as part of the SPUR Phase I Conceptual Design and described in the previous section, was based on a twelve-month schedule for design, development, and evaluation of critical circuits of the optimum processor. During the third and fourth months of the contract, the validation effort was redirected to meet a five-month schedule. The results of this reduced effort are reported upon herein.

The major changes of the program were a) a reduction of the effort in all tasks, such that actual hardware tests were performed on only one unit, the Post Filtering Processor, b) the elimination of the detailed design of the two-step flash A/D converters and the fault detection circuitry of these units, and c) elimination of the verification of the Zero Channel Processor.

The detailed results in each processor functional area are discussed in the next five sections.

4.1 ANALOG AND A/D PROCESSING FUNCTION

In the Validation Program for the Analog and A/D Processing Function, the dc offset correction loop was designed as an example of automatic testing and calibration of analog circuits. This design was selected because the need for automatic calibration circuitry for the A/D converter was recognized as a key feature of future unattended radars. Drift in uncorrected systems can be relatively large; for example, during recent operation of the ITTG L-band demonstration radar, dc offset voltages were measured as high as ± 200 mV. With the installed 10 bit A/D converter (9 bits + sign) this drift corresponds to affecting 4-5 bits at the output. Dynamic range is thereby effectively reduced by the offset voltage. Another major effect occurs on systems with hard-limited pulse compression since they operate on the MSB of the converter which is changed by the code or toggled by noise. When drift introduces a bias at the input to the A/D converter, the noise statistics no longer have an expected value (mean) of zero, with the result that time sidelobes are increased, thereby degrading performance.

In order to verify the performance of a dc correction loop, the unit was designed to perform the automatic calibration function for the ITTG L-band demonstration radar A/D converter system.

The L-band demonstration radar uses a single high speed converter to digitize both the I and Q channels to 10 bits each. Hence the two channels of video from the receiver are time multiplexed into the converter, converted, and demultiplexed into separate I and Q registers. From these, the digital words enter the demonstration processor.

The addition of the correction loop to the processor was accomplished by replacing the existing interfacing circuitry between the A/D converter and the processor with new circuitry adding the correction loop, upgrading the interface between the A/D converter and the processor, and adding an additional interface to the A/D converter. This additional interface, Processor B interface, was provided to allow the SPUR Doppler Filter Modules to be integrated into the radar.

The automatic calibration circuits monitor the sign bits of the I and Q channels of either the A or B interface. Consider the Q channel of the monitored interface for further discussion. Over a selected number of sweeps, involving n range bins, a counter accumulates the quantity $P-N$, where P = number of positive signs, N = number of negative signs. This quantity, $P-N$, will be close to zero when there is no dc offset. If $P-N$ is significantly different from zero, the calibration circuit increments/decrements a Correction Register. The contents of this register, converted to an analog quantity in the $\pm 5V$ range and called the Q Calibrate Level, is sent to the receiver where it is scaled and used to adjust the Q channel dc level. Thus the contents of the Correction Register, times a scale factor, equals the effective correction level at the input to the A/D Converter. An additional check of the circuitry is provided by comparing the contents of the Correction Register to preset positive/negative limits based on expected drift. If the calibration level is excessive, an error light is lit and an out-of-tolerance strobe is provided. This flag can be used for error detection by the STATE Processor, for example.

The detailed design of the principal board in the modification of the A/D converter system, the A/D Interface (ADI) Board, has been completed. A block diagram of the modified system is given in Figure 4-1, while Table 4-I provides the required performance parameters as the correction loop function. A programmable architecture was chosen for the A/D I board. This choice allows for some experimentation and optimization of parameters. Operation of the unit, considering a single channel, is described in the following paragraphs (refer to Figure 4-1).

The receiver produces I and Q signals consisting of a random component and a fixed component (dc offset). The fixed components are to be nulled out by the correction voltages developed by the A/D I Board. The signals plus initial correction voltages (which can be assumed to be zero) form the I and Q bipolar videos sent to the A/D Converter.

The signs of the digitized data words are accumulated in counters: positive causes an upcount while negative causes a downcount. After n range bins, the accumulated count divided by the number of samples, n , is assumed to be normally distributed (using the Central Limit Theorem of Probability). When the count at the end of the collection interval is positive, the Correction Register is incremented. When the count is negative, the Correction Register is decremented. The contents of the Correction Register, after updating, are converted to an analog correction voltage by the output D/A converter. This analog result is scaled in the receiver and used to adjust the dc level of the receiver video amplifier of the appropriate channel. Two independent loops operate on the two channels (I and Q).

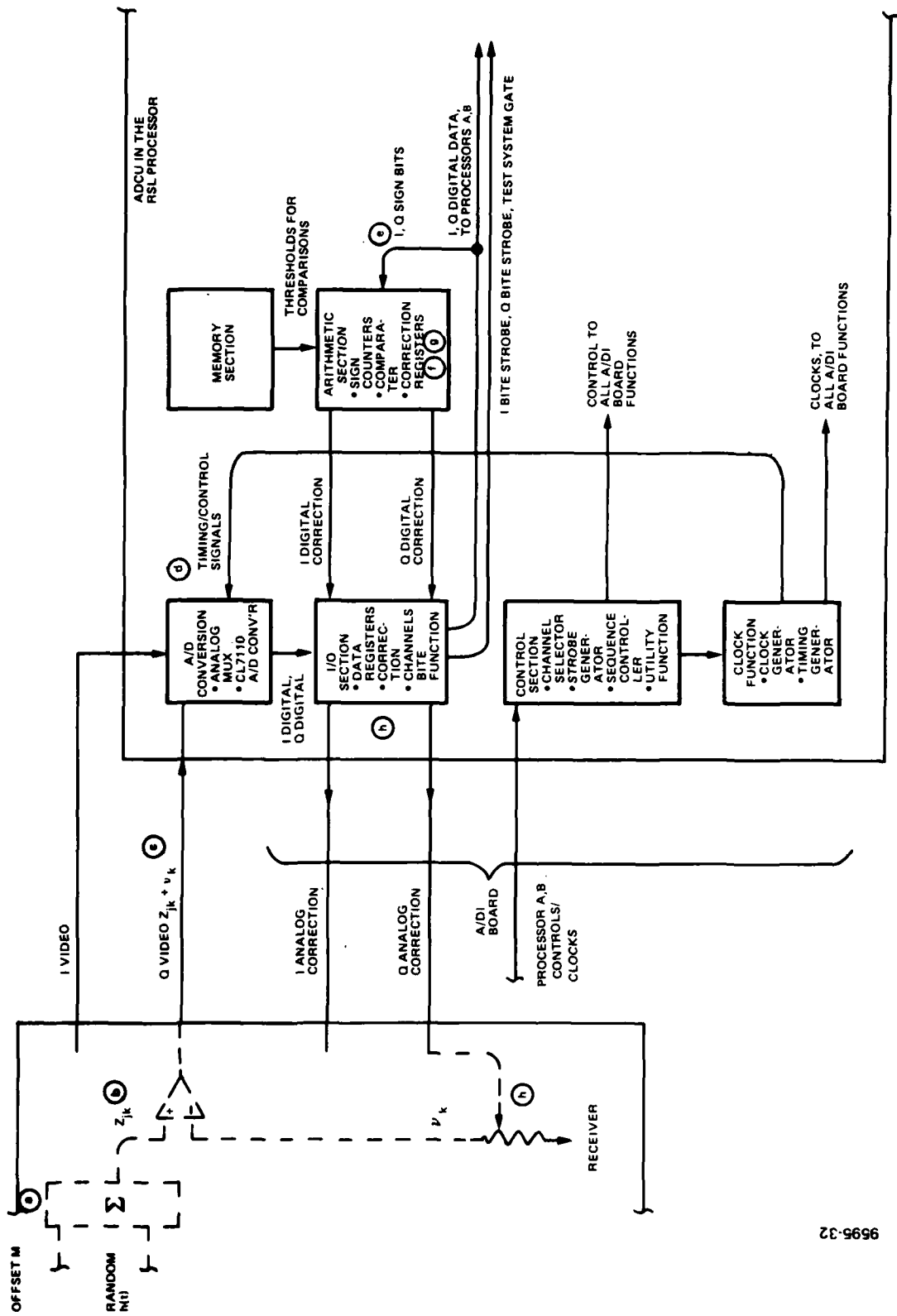


Figure 4-1. Block Diagram of Upgraded A/D Converter in the ITT Gilfillan Demonstration Radar

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Table 4-I. Required Performance Characteristics

<u>Parameter</u>	<u>Requirement</u>
Frequency	to 2.6 MHz
Calibration Levels, I, Q:	to ± 2047 quanta
Quanta Sizes:	adjustable; at the A/D converter unit input, from 10 mV down to 10/8 mV.
Data Collection Intervals:	16 choices can be programmed
BITE Data Reporting:	out of tolerance signals for the calibration levels; visible LED's
Unit Test Capability:	TEST SYSTEM gate generated from RUN/TEST switch
Maximum Sweep Interval:	approximately 4K range bins/sweep

The dc correction loop is designed to correct drift and hence has a long time constant. Only one count change is allowed per data collection interval. The response time for the loop for a full scale input change is about 25 seconds. The resulting uncompensated offset can be held to less than one LSB according to preliminary analysis of the loop. The compensation loop design is also independent of the number of bits of the A/D converter system (since it operates only on the sign bit) and hence is applicable to the recommended 11 bit converter of the SPUR.

The detailed design of the calibration loops for the I and Q channels totals 65 integrated circuits in the programmable demonstration design. The estimated power is 6.5 watts and the failure rate of the loop is estimated to be 3.77 failures per 10^6 hours. However, the loops are within the redundant portions of the A/D converter and therefore contribute less than 0.1 failures per 10^6 hours to the system.

The calibration loop as presently configured is a generalized design developed for maximum flexibility and proof of concept. A recommended design, based on testing this unit in the system, is estimated to require only 50 to 60 percent of the integrated circuits of the current design. This estimate is based on the replacement of many programmable features of the design, such as threshold levels and data collection intervals, with fixed designs and the simplification of the interfacing to a single processor. The reduced design allows the A/D converter system to fit on one board as estimated during the SPUR Phase I Design.

4.2 DOPPLER PROCESSING FUNCTION

In the validation program for the Doppler Processing Function, the Doppler Filter Modules were selected for detailed design and the pulse compression system was recommended for implementation. The module design is discussed herein and the pulse compression system is discussed in Section 4.2.2.

4.2.1 Doppler Filter Modules

Two methods of organizing the Doppler Filter Modules were identified in the Phase I final report for SPUR. These methods were:

- Range Block Doppler Module (RBDM)
- Doppler Filter Module (DFM)

In the RBDM organization, each module performed the required calculations to implement all six near-optimum FIR filters for a block of ranges. Four Range Block Doppler Modules were provided, of which three were on-line and one was unpowered in an off-line (spare) mode.

In the DFM organization, each module contained two filters, either one of which could be used to implement any one of six near-optimum FIR filters for all range bins. Eight Doppler filters were provided, of which six were on-line and two were unpowered in an off-line mode.

The results of the trade studies showed that neither organization had a clear advantage over the other. The RBDM was initially selected, however, because the RBDM was easier to test in an experimental radar than the DFM. A single RBDM module develops all of the Doppler Filters for a block of range bins and, therefore, less units would be required for testing.

During the initial design activity of Phase II, it was determined that the RBDM could not be packaged on a single 14 by 15 inch logic board, as originally planned. (The RBDM exceeded the capacity of the board by approximately 20 percent.) As a result, the detailed design of the DFM was initiated at that point. The remainder of this section describes the design of the Doppler Filter Modules.

Doppler Processor Subsystem Description

The major functional characteristics of the SPUR Doppler processor subsystem are provided in Table 4-II. A block diagram of the subsystem is provided in Figure 4-2.

As shown in Figure 4-2, the subsystem is configured using four identical Doppler filter modules. Each module is packaged on a single 14 by 15 inch logic board. Each module contains two Doppler filters. Four system buses are used for communication of data and control. An Input data bus provides A/D converter data to each of the four DFMs at

Table 4-II. SPUR Doppler Processor Subsystem Characteristics

Doppler Filtering Approach	Narrow band filter bank
Number of Filters Provided	6
Filter Type	Finite Impulse Response ("near-optimum" filter transfer functions implemented using PROM resident weights)
Range Coverage	550 range bins (1024 range bins provided)
Range Sampling Interval	618 nanoseconds (1/20 nmi) (2 samples per range bin)
Input Data	Complex, sign + 10-bits
Processing	
Multiplications	Complex, S + 11-bits
Accumulations	Complex, S + 15-bits
Output Data	Complex, hard-limited, Sign-bit only
Built-in-Test	Input data parity, input port for test data, output port for test data, output buffer memory checksum
Redundancy	2 standby redundant off-line filters provided

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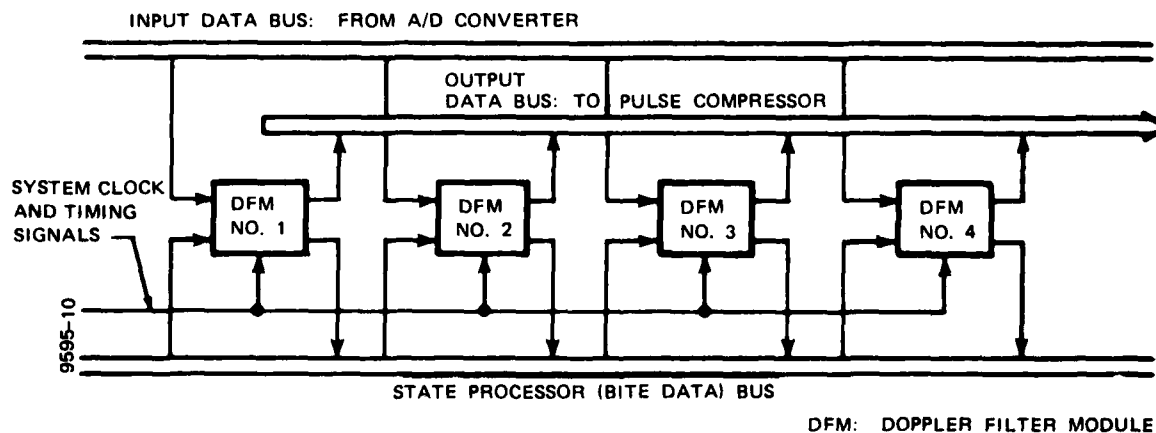


Figure 4-2. Spur Doppler processor subsystem block diagram

the rate of one complex sample each 618 nanoseconds. An Output data bus provides hard limited filter output data from the four DFMs to the Pulse Compressor at the rate of one complex output sample each 618 nanoseconds. A STATE Processor BITE data bus provides test target input data to each of the four DFMs and receives test target output data from each of the four DFMs. In addition, the STATE Processor provides filter weight set selection (selection of one of two sets of weights) to all of the DFMs and filter addresses (to the DFM which is designated as the standby redundant unit) over the STATE processor BITE data bus. The system clock and range gated timing signals are provided to the four DFMs from a central system timing unit.

Doppler Filter Module Description

The Doppler filter module (DFM) contains all of the processing circuits necessary to implement two finite-impulse-response (FIR) filters. Each of the two filters on the DFM uses separate and independent processing circuits. However, certain control, interface, and BITE support functions are shared between the two filters and these common functions are accordingly provided by a common set of logic circuits. The Unit Design Requirement (UDR) for the Doppler Filter Modules is given in Appendix B.

Doppler Filter Address Modes

Each doppler filter is provided with an identical set of filter weights which are stored in a weight memory PROM. This PROM is addressed by an eight-bit field consisting of a 3-bit filter address field, a 3-bit interpulse period address field, a 1-bit real/imaginary component select field, and a 1-bit weight set select field. Filter address fields are brought out to the board edge connector for each of the four DFMs. Six of the eight filters have their addresses programmed through the board edge connector by their slot position in the back plane. The address fields for the other two filters are jumpered to the filter address pins on the board edge connector. These latter pins contain address data sent to that module from the STATE Processor over the STATE Processor Bus.

This addressing technique provides for establishing six unique Doppler filters having preset addresses and two addressable Doppler filters with addresses under control of the STATE processor. It also provides for the STATE processor to switch all eight filters to one of two sets of weights.

Interface Description

Interface descriptions are provided in Table 4-III for each of the four buses which form the external interfaces of the DFM. These buses are:

- Input Data Bus
- Output Data Bus
- STATE Processor Bus
- Timing and Control Bus

Table 4-III. Doppler Filter Module (DFM) Interface Descriptions

	<u>Number of Lines</u>	<u>Comments</u>
<u>Input Data Bus</u>		
I-Data	(12)	Sign + 10-data + Parity
Q-Data	(12)	Sign + 10-data + Parity
<u>Output Data Bus</u>		
Filter F1	(2)	Sign [Re] + Sign [Im]
Filter F2	(2)	Sign [Re] + Sign [Im]
<u>State Processor Bus</u>		
Data	(3)	Bi-directional, majority logic Note: Formats given in Figures II, III
Input Shift Control	(1)	Note: Formats given in Figure II
Output Shift Control	(1)	Note: Formats given in Figure III
<u>Timing and Control</u>		
618 nanosecond Clock	(1)	
309 nanosecond Clock	(1)	
Write Enable Pulse	(1)	
Live Time	(1)	
Interpulse Period Zero	(1)	

The input and output data buses provide data at the range sampling rate of 618 nanoseconds. The STATE Processor Bus consists of three bidirectional data lines which are operated in a fault tolerant 2 out of 3 mode and two control lines: an Input Shift Control and an Output Shift Control. Data is shifted to and from the DFM under control of the STATE Processor. The format of the input data received from the STATE Processor is given in Figure 4-3. The format of the output data sent to the STATE Processor is given in Figure 4-4. Input data must be received at the DFM by the start of live time for each of the eight PRIs in an azimuth group for which data is processed. Output data is valid and may be requested by the STATE Processor any time following the azimuth group for which it was calculated.

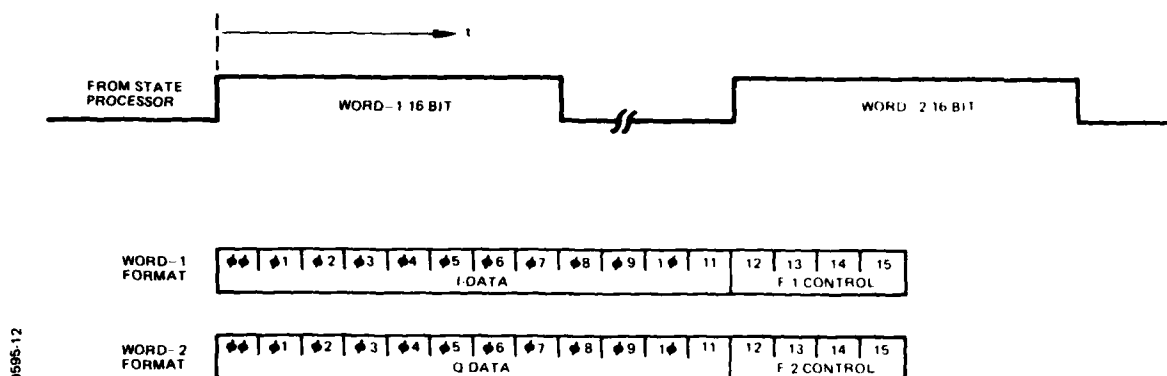


Figure 4-3. Input Data Formats for the STATE Processor Bus

System Timing

The worst case system timing for the SPUR Doppler Processor is given in Figures 4-5 and 4-6. Figure 4-5 establishes the minimum time for a nine PRI azimuth group of 7209 μ secs. Data is collected by the DFMs and processed in real time during the last eight PRIs of the nine PRI interval. As data samples are collected, the complex sample for each range interval is multiplied by the complex weight for that PRI and filter address and the product is accumulated to form a sum of products in each of the six filters for each of the 1100 range sampling intervals. Filter data is loaded into the output memory during the PRI number eight for each filter at an address specified by the given range sampling interval. As shown in Figure 4-6, the contents of the output memory are presented on the Output Data Bus eight times — once during each of eight PRIs. Output filter data may then be processed by the Post-Filtering Processor in any order that is convenient. Data from a redundant Doppler filter is simply selected instead of the data from the filter which it is replacing.

DFM Block Diagram

A simplified block diagram of the DFM is provided in Figure 4-7. A common input section selects between a 24-bit input data sample from the Input Data Bus and a 24-bit BITE data sample. Common timing and control, output memory, bit generation and output registers are provided. Each doppler filter consists of a PROM multiplier-accumulator section and an input memory accumulator section.

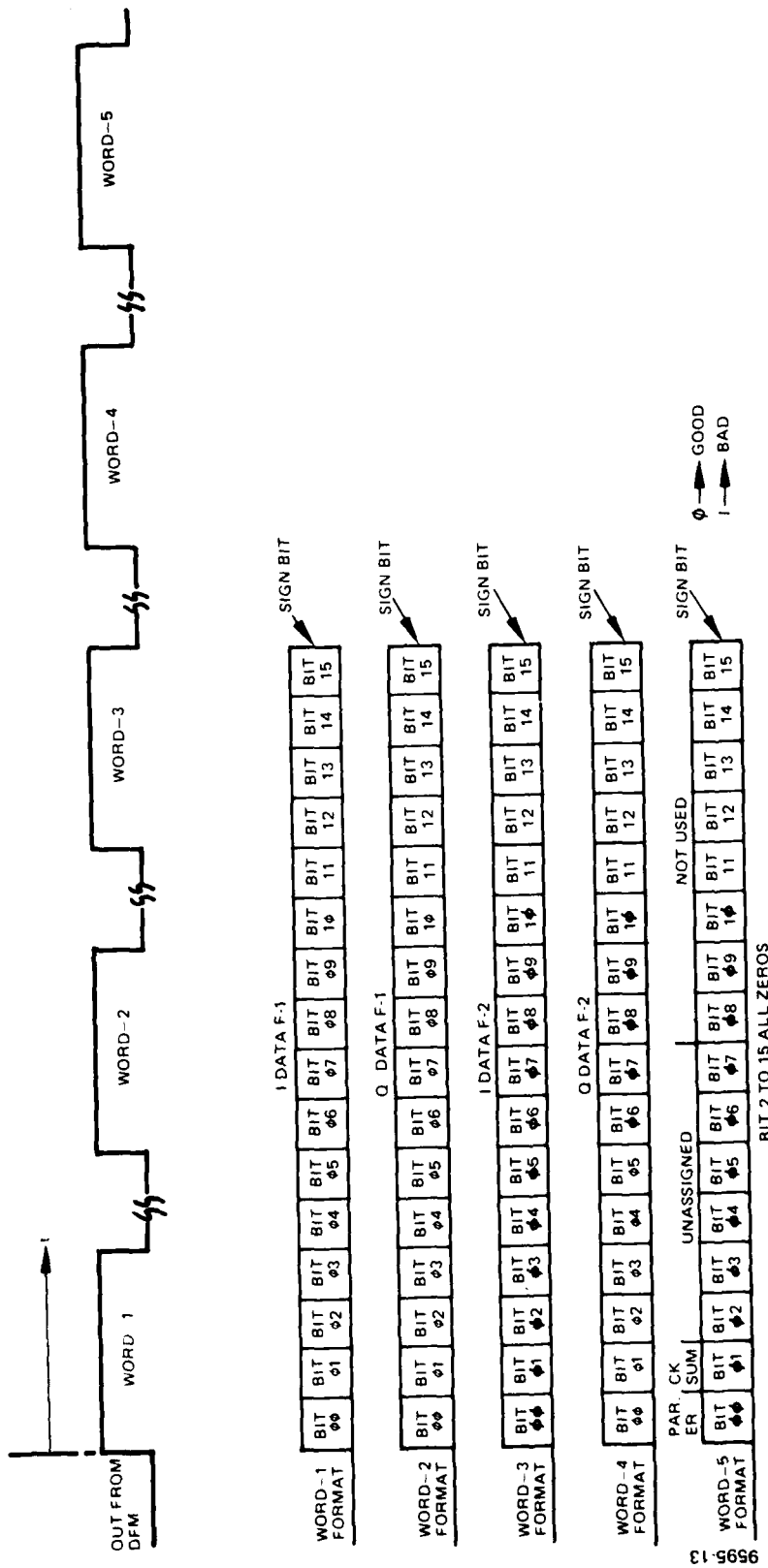


Figure 4-4. Output data formats for the STATE Processor Bus

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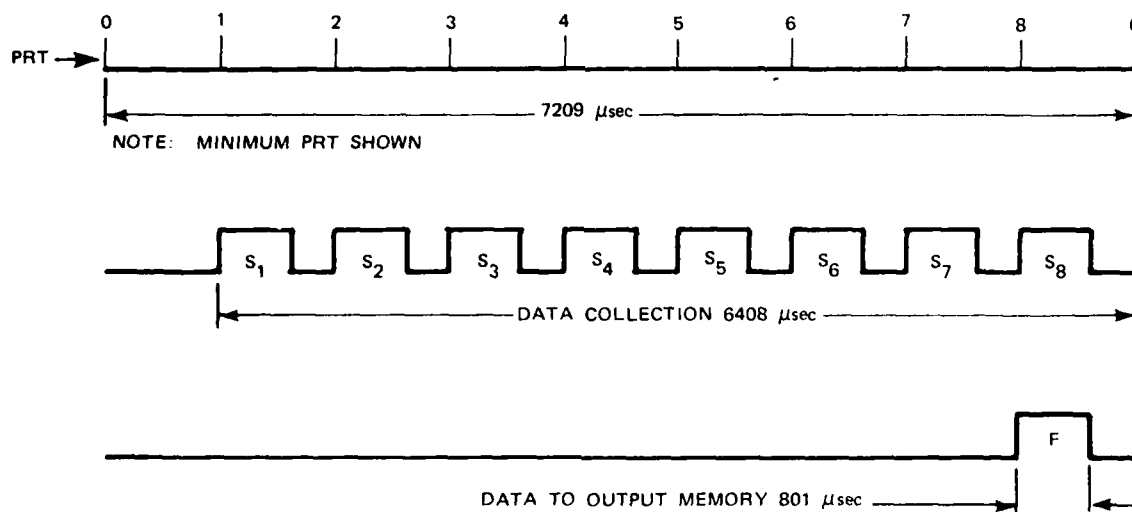
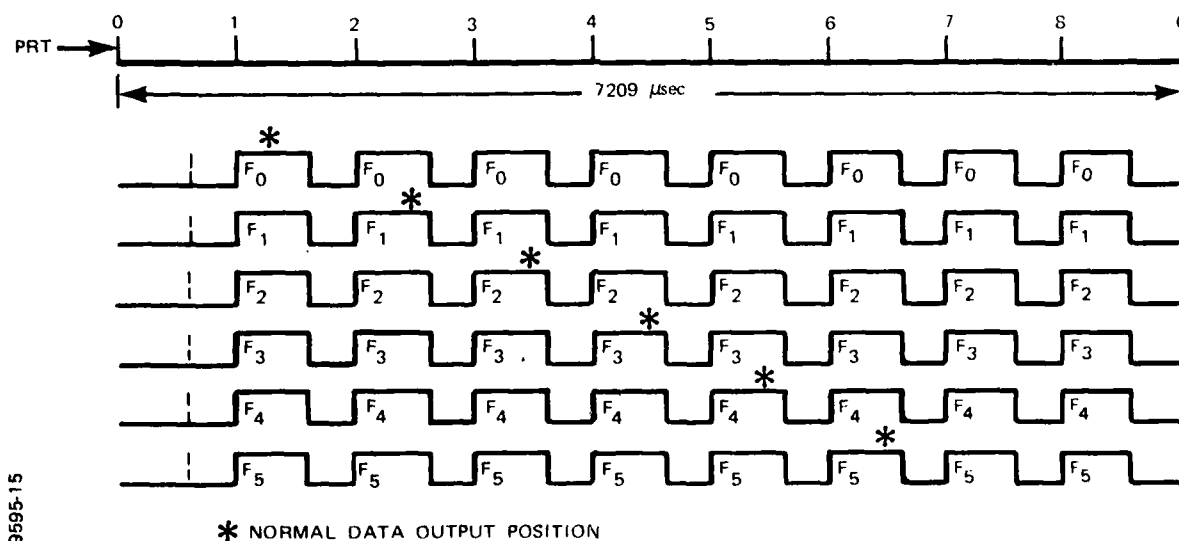


Figure 4-5. I/O data sequences of DFM



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Figure 4-6. Output from output memory

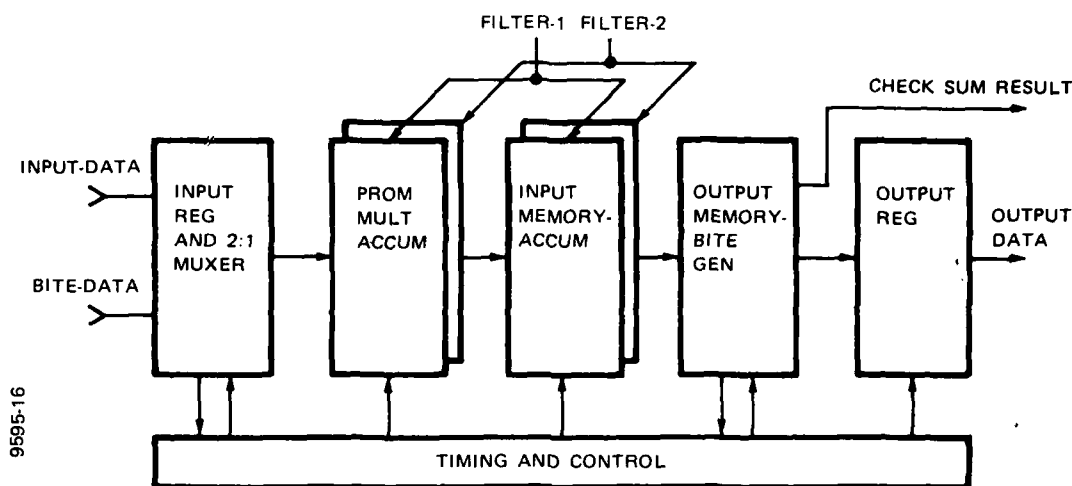


Figure 4-7. Functional block diagram of a DFM
(Two filters in the module)

The output of the common input data register is provided to each of the two Doppler filters.

Input Data Selection

The input data selection logic contains a 24-bit input data register and 2:1 input multiplexer. This section also contains a 32-bit shift register and an 8-bit filter address register. The 32-bit shift register is loaded by the STATE Processor with 24-bits of test data and 8-bits of filter address control data immediately prior to the start of live time for each PRI for which data is to be processed. The address control data is transferred to the 8-bit filter address register only at the start of PRI 1 in each azimuth group. (Preset filter addresses are loaded into the control registers at that time for the three DFMs which are not address programmable.)

Test data is selected for processing during the first 618 nanosecond range sampling interval immediately following the 1100 range sampling intervals of live time. During live time, data from the Input data bus is selected.

The 24-bit output of the input data register is provided to two 12-bit multiplexers. These are used to form two 12-bit paths: a first multiplicand path which goes to the real component multiplier-accumulator in each of the two filters and a second multiplicand path which goes to the imaginary component multiplier-accumulator in each of the two filters.

These multiplexers are used to time-division-multiplex the real and imaginary components of the input data register during alternate 309 nanosecond clock periods onto the complex multiplicand data path.

Parity of the multiplicand data path is tested and the results latched during each range sampling interval.

PROM/Multiplier-Accumulator

Each filter has its own PROM/multiplier-accumulator. This section contains a complex multiplier which is capable of multiplying a complex input multiplicand (Sign and 10-bit real, sign and 10-bit imaginary) by a stored complex multiplier weight (sign and 11-bit real, Sign and 11-bit imaginary). The complex multiplication for each filter is performed in two 12-bit by 12-bit LSI multiplier-accumulators (one real, one imaginary) over two 309 nanosecond clock periods. During the first clock period, each component of the complex input multiplicand is multiplied by the imaginary component of the stored multiplier weight; during the second clock period, each component of the complex input multiplicand is multiplied by the real component of the stored multiplier weight and combined with the product formed on the previous clock. This complex sum is then rounded to two 12-bit numbers and sent to the input memory/accumulator section for that filter.

The complex multiplier weights are stored in a 256 word by 12-bit PROM. The PROM is divided into two weight sets of 128 words each. Each weight set consists of 64 complex weights, 48 of which are used to generate the six filters. The 64-weights are addressed by the 3-bit filter address field which is unique to each filter and the 3-bit PRI field which is a function of the pulse repetition interval counter in the timing and control section. Weight set selection is controlled by the STATE Processor.

Input Memory/Accumulator

Each filter contains its own input memory/accumulator section. This section contains a 2K-word by 32-bit input memory and two 16-bit accumulators. The contents of the memory are set equal to the output of the PROM multiplier-accumulator during PRI number one. During the next seven PRIs, the complex products from the PROM/multiplier-accumulator are summed for each range sampling interval. The running sum is read out of the input memory, added to the latest weighted product and returned to the input memory. The memory is accessed each 309 nanoseconds. One read cycle and one write cycle are performed each 618 nanoseconds.

During PRI number eight, the sign bits of the real and the imaginary components of the filter are sent to the output memory. During test target time of PRI number eight, the 32-bit complex product of each filter is strobed into a 32-bit BITE data shift register. This data is later shifted onto the STATE Processor data bus under control of the STATE Processor.

Output Memory/Bite Generator

This section contains a 2K-word by 8-bit output memory. Four of the 8-bits are used to store the hard-limited data from each of the two filters. (The other 4-bits are not used.) Data is written into the output memory during PRI number 8. Data is read out of the output memory during PRI numbers 1 through 8. Data from the output memory is sent to the 4-bit output register where it is clocked onto the Output data bus at the range sampling rate of 618 nanoseconds.

A checksum is generated during the time that data is being written into the output memory. Each time that data is read from the output memory, a new checksum is computed and compared with the original value. The results of the comparison are latched and reported to the STATE Processor over the STATE Processor data bus.

Timing and Control

This section provides clocks, required range gated strobes, and addressing and control for the weight PROM, input memory, and output memory.

Built-in Test Summary

Input data parity is tested prior to loading of input data into the multipliers. Test data is received from the STATE Processor, processed immediately following live time, and returned to the STATE Processor for verification. Checksums are generated for the output memory. Parity test results and checksum test results are reported to the STATE Processor.

Power Consumption

The predicted power consumption (based on the detailed design) for a single DFM is 32.8 watts. This result is 15.8 watts per board below that predicted for the DFMs in Phase I, because the memory chip selected for the detailed design uses considerably less power than the one used in the Phase I predictions. However, this power is still 7.7 watts per module higher than the predicted RBDM value. Additional power could be saved by restricting the number of range sampling intervals to 1024, thereby deleting half of the memory on the board. This change would reduce the power estimate to 28.9 watts per board.

Reliability

The predicted failure rate for the four DFMs operated in a six-filter out of eight-filter configuration is conservatively estimated at 9.85 failures per 10^6 hours. The estimate is conservative because all boards are assumed powered for this calculation. This result is 2.61 failures per 10^6 hours higher than the estimate for the RBDM implementation and 4.44 failures per 10^6 hours higher than the Phase I DFM estimate. This increase is directly attributable to the necessity of utilizing common logic for some parts of the control of the filters. The failure rate can be reduced to 4.74 failures per 10^6 hours if the number of range sample intervals is reduced to 1024, thereby deleting half of the processor memory. This change could be accomplished by increasing the minimum range to 8.8 nmi, or by increasing the range bin size by 7 percent.

4.2.2 Post-Filtering Processor

The Post-Filtering Processor consists of a.) hardlimited, binary phase-coded pulse compression implemented in a novel way to reduce losses due to target Doppler velocity, and b.) range combination to reduce the double-sampled, envelope-detected video to a single sample per range bin (see appendix C). The Validation Program consisted of designing and fabricating a partial board which was interfaced to a modified, existing pulse compression board; the two board combination was partially integrated into the L-band demonstration radar for operational tests on the pulse compression portion of the PFP. The range combination circuitry was fabricated but no quantitative data was taken on its performance beyond operational verification and power measurement.

During the Phase I Conceptual Design, hardlimited, binary phase-coded, pulse compression with Doppler compensation in the form of three effective channels covering the target Doppler velocities was judged the optimum pulse compression method for the SPUR. The new implementation of generating three channels after partial pulse compression (described below) retains the relatively inexpensive binary, phase-coding approach while substantially reducing the signal-to-noise ratio (S/N) losses normally suffered against targets with large Doppler velocities. In the SPUR, the compensated pulse compression system was calculated to reduce the S/N loss from 2.5 dB to 0.9 dB (worst case) against a 2400 knot Doppler target. This loss included the actual Doppler sensitivity loss of 0.6 dB and a channel collapsing loss (3:1) of 0.3 dB. Loss curves for the single channel and three channel processes are shown in Figure 4-8.

Post-Filtering Processor Functional Description

The PFP performs eight functions:

- Preliminary Pulse Compression
- Zero Channel Addition
- Positive Doppler Channel Rotation
- Negative Doppler Channel Rotation
- Envelope Detections
- Greatest-of-Selection
- Range Combination
- BITE

A simplified block diagram of these functions (Figure 4-9) also illustrates the functions resident on the existing board and the new board. The input to the PFP is from the DFM's discussed in the previous section. An 8:1 multiplexer at the input selects the hard-limited complex data from the appropriate filter to be compressed during a given PRI under the control of the STATE Processor. This data is compressed in two sections: a first half 15-bit section and a second half 16-bit section. This compression is the Preliminary Pulse Compression. To form the normal zero channel the two halves are added together and envelope-detected using the approximation $(\max(I,Q) + 1/4 \min(I,Q))$. To form the positive and negative Doppler channels, the I and Q data from the second half is rotated

THREE-CHANNEL PULSE COMPRESSION

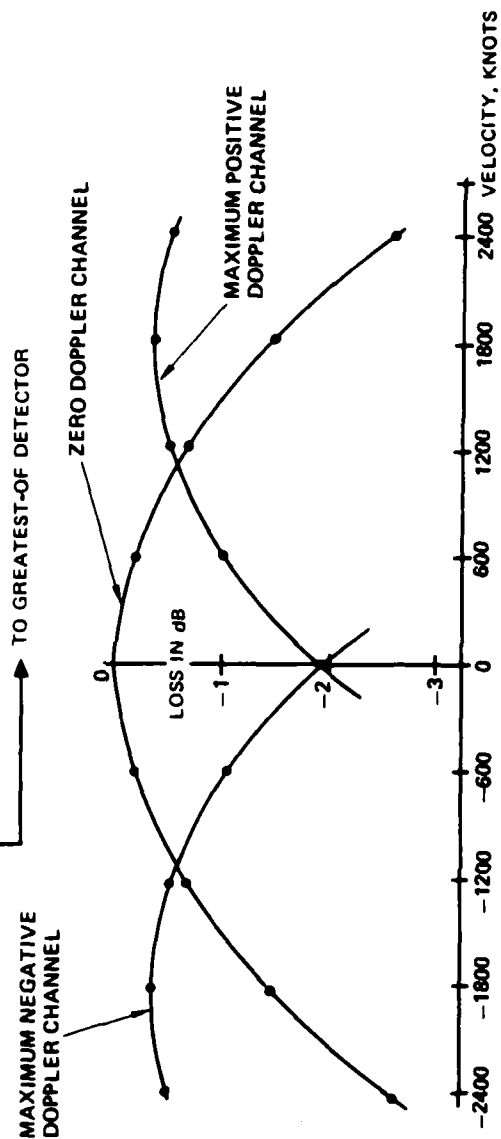


Figure 4-8. Using three channels for pulse compression reduces signal-to-noise ratio losses.

9695-34

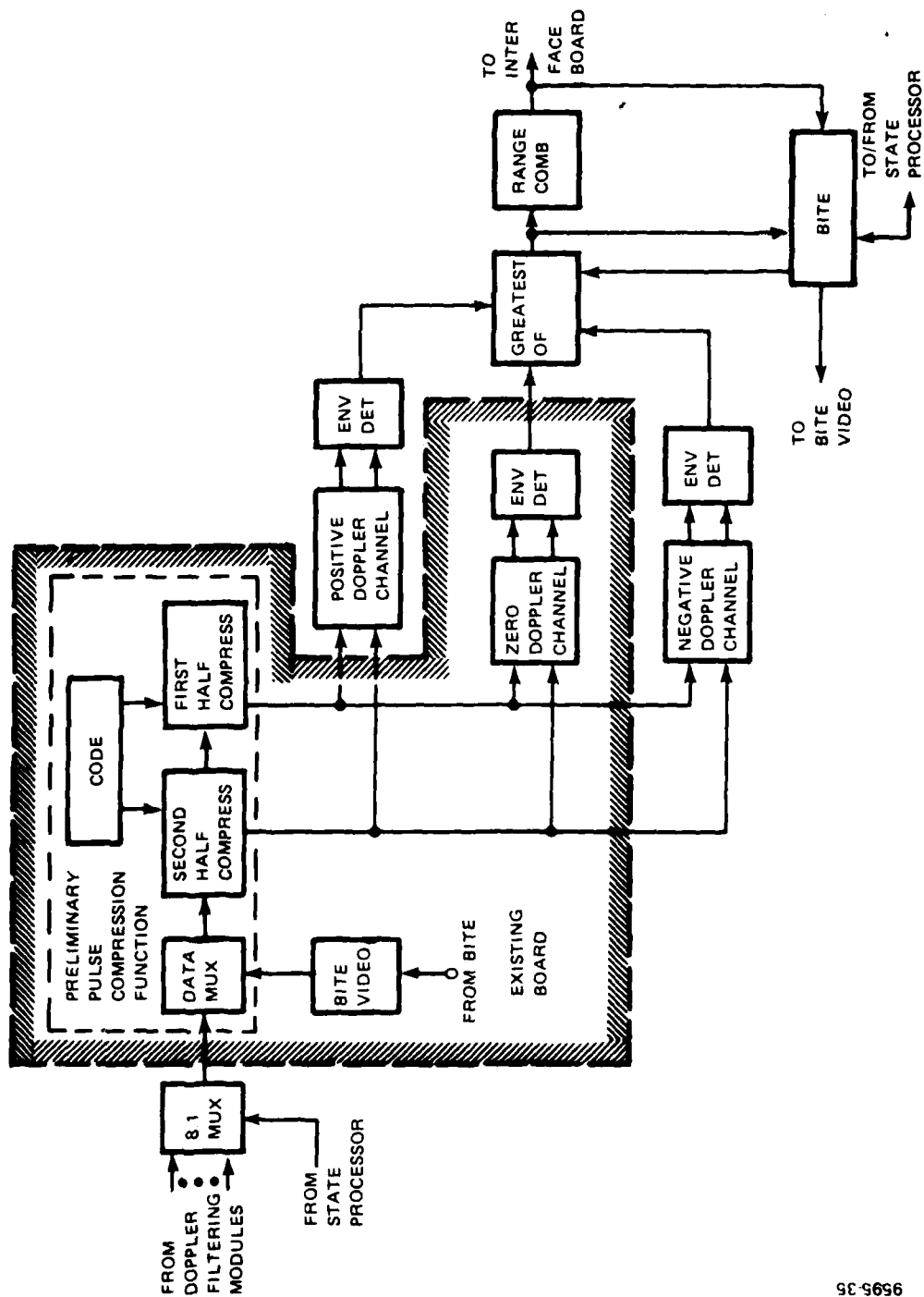


Figure 4-9. Simplified Post-Filtering Processor functional block diagram

9595-35

to be in phase with the data from the first half by the approximation to a complex multiply ($I'_2 + jQ'_2 = (0.25 \pm j 1.0)(I_2 + jQ_2)$). The rotated I and Q data is then added to the first half I and Q data and the result is envelope-detected in two detectors using the same approximation as in the zero channel. The Greatest-of-Selection Function selects the channel with the maximum amplitude for further processing. The Range Combination Function adds the odd data samples to the even data samples ($R_i + R_{i+1}$, i odd) to produce one data sample per range bin (1.236 μ sec). The output data is parity-encoded and sent to the Interface Board for threshold detection and multinomial integration. The BITE Function provides BITE video for test of the pulse compression channels, evaluates BITE signals at the output of the Range Combination Function, and controls the Greatest-of-Selection should a failure occur in a single channel. The basic BITE test is a perfect code input which, after being decoded, is compared to thresholds calculated for each channel.

Post-Filtering Processor Implementation

As previously mentioned, the PFP was implemented on two boards: the modified p/c board and the new board. The modified p/c board contains the preliminary pulse compression function, the zero channel and envelope detector, and the BITE circuitry. It differs from the recommended SPUR design in that it uses a six-level adder tree to perform the pulse compression, while the SPUR system recommends PROMs for the first three levels and adds thereafter. In addition, the SPUR recommendation is to use LS TTL whereas the existing design uses mainly Schottky and regular TTL. With these differences, the validation of power and reliability required a combination of measured and estimated values.

The new PFP board forms the Negative and Positive Doppler Channels with envelope detections, performs the Greatest-of-Selection Function, and performs the Range Combination Function. This board is implemented entirely in LS TTL.

A summary of the two board designs is given in Table 4-IV. The existing board design utilizes approximately half of the 14 X 15 inch board area. The new board design also uses approximately half of a 14 X 15 inch board area. Thus, a final design of the PFP will fit on a single 14 X 15 inch board as originally estimated during the Phase I Conceptual Design.

Post-Filtering Processor Test Results

For functional validation tests the two boards were integrated into the L-band demonstration radar by bringing the sign bits of the 10-bit A/D converter to the existing board, using the system clocks, and providing output data to the system display interface board (D/A converter). The basic clock rate for the pulse compression board in the system is 10.36 MHz, because it is a time multiplexed design. After Preliminary Pulse Compression when the I and Q data are demultiplexed, the rate drops in half to 5.18 MHz. The new board was run at 5.18 MHz because of its position in the processing. Thus the pulse compression system was tested using a clock three times faster than the SPUR clock. The range bin or compressed pulse width for all testing was 0.386 μ sec. The code length was the design 31 bits giving an uncompressed pulsewidth of 12 μ sec.

Table 4-IV. Post-Filtering Processor Validation Boards

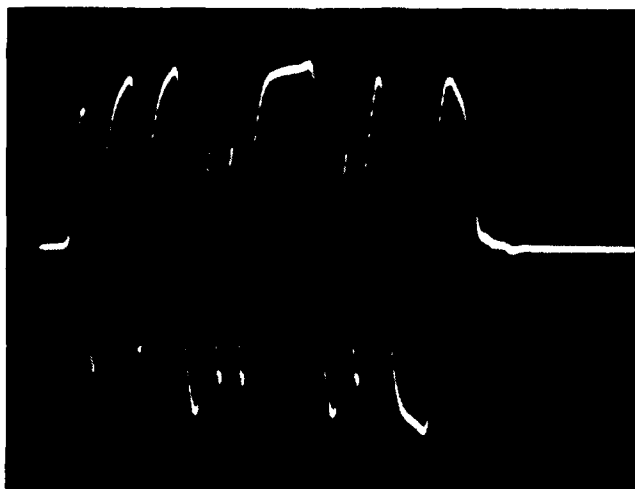
	<u>Existing, Modified Board</u>	<u>New Board</u>
Functions	Preliminary Pulse Compression Zero Channel Envelope Detection BITE	Negative Doppler Channel Positive Doppler Channel Envelope Detections (2) Greatest-of-Selection Range Combination
Board Size	14 X 15 inch	14 X 15 inch
No. of IC's	90	102
IC Technology	Schottky TTL and TTL	Low Power Schottky TTL
Wiring	Multiwire	Wirewrap
Power supply	+5V	+5V
Power (measured)	21 watts	6 watts

To form the input signal for decoding, the frequency synthesizer output at L-band was coupled to the frontend of the receiver. This arrangement provided a fixed target at zero Doppler for evaluation. The Q channel coded video at the input to the A/D converter is shown in Figure 4-10. The sign bit of the A/D conversion of this signal is sent to the pulse compressor.

Operation of the pulse compression system at zero Doppler was verified. The input video and compressed pulse after D/A conversion are shown in Figure 4-11 for the zero channel. The position of the compressed pulse is due to the delay inherent in the processing. Sidelobes are visible only on the right side of the compressed pulse because a display gate has eliminated any video displaced further than 2 μ sec to the left side of the compressed pulse. This gate is a system feature preventing display of video at transmit time. The output of the pulse compressor in all channels was as expected (i.e., correct value of peak as measured with a logic analyzer after envelope detection but before D/A conversion). The peak value of the Zero Channel was 38 counts, while the offset channels were 35 counts. A qualitative comparison of the sidelobe level degradation due to the three channels passing through the Greatest-of-Selector (GOS) is shown in Figure 4-12. Figure 4-12a is the zero channel output video measured with the GOS set to only pass the Zero channel. Figure 4-12b, however, illustrates the increased sidelobes when the GOS is set to perform its normal operation.

A simple analysis was performed to estimate the effect of the selection of maximum sidelobes through the three-channel pulse compressor. The worst case sidelobe, occurring at a Doppler offset of 4200 knots from the center of a filter (see Figure 4-8), has an amplitude of 10.25 (after the envelope detector approximation of $\max \{|I|, |Q|\} + \frac{1}{4} \min \{|I|, |Q|\}$) when a fully correlating signal is present in both I and Q channels (i.e., signal phase = 45°). Since the gain, through the pulse compressor, for a noise signal is $\sqrt{31}$ and the gain for a coherent

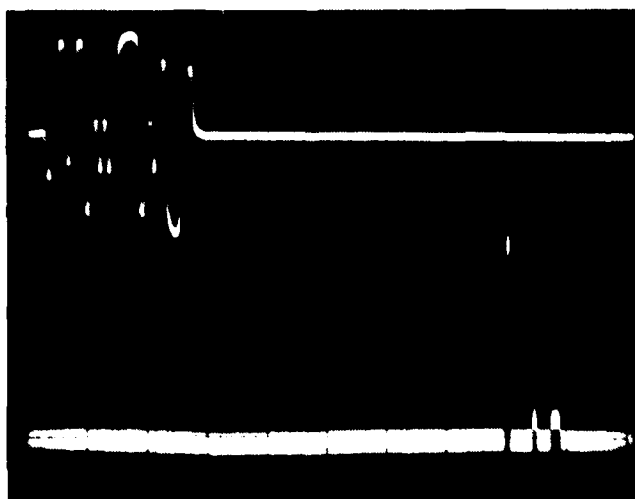
9595-37



SCALES =
VERTICAL
1.0 v/div
HORIZONTAL
2.0 μ sec/div

Figure 4-10. Q channel analog coded video at the input to the A/D converter.

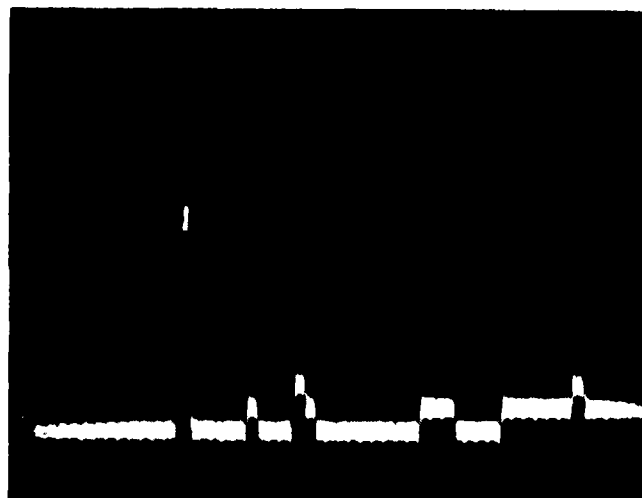
9595-38



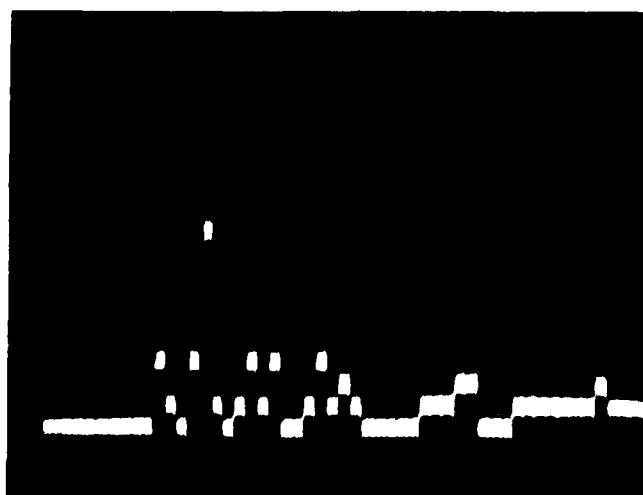
SCALES =
VERTICAL
CHANNEL 1
2.0 v/div
CHANNEL 2
0.5 v/div
HORIZONTAL
5.0 μ sec/div

Figure 4-11. Uncompressed input coded pulse and output compressed pulse.

9595-39



a) ZERO DOPPLER CHANNEL



b) AFTER GREATEST-OF-SELECTOR

SCALES =
VERTICAL
0.5 v/div
HORIZONTAL
2.0 μ sec/div

Figure 4-12. Zero channel compressed pulse.

signal is 31, the dynamic range at the output of the compressor is limited to about 15 dB ($20 \log \sqrt{3T}$). At the output of the envelope detector, a fully correlating signal attains an amplitude of 38.75. The noise level, therefore, is 6.93.

To perform the analysis, the presence of a worst case sidelobe is modeled as a signal-plus-noise case; the distribution of this case is Rician. However, for this simple analysis, a Gaussian approximation to the Rician distribution was used. Therefore, the density of the signal at the input to the multinomial detector is Gaussian with mean 10.25 and standard deviation 6.93.

The multinomial detector is a dual threshold process. The first threshold generates a two-bit representation of the input signal (by using three subthresholds) while the second threshold, operating on the sum of four of the results of the first threshold, generates the detections. The multinomial detector has been analyzed by Hansen.¹ Subthreshold values of 13.79, 20.54, and 25.68, and a second threshold value of 7 correspond to the SPUR case of $P_d = 0.90$ and $P_{fa} = 10^{-5}$. These values were estimated from the threshold values given in the above work.

Given the input distribution and the characteristics of the ATD, the P_d due to a sidelobe can be calculated. The probability of crossing each threshold is calculated in the usual manner using the erf:

$$P \{ X > V_i \} = 1 - \text{erf} (V_i) = 1 - \int_{-\infty}^{V_i} \frac{1}{\sqrt{2\pi}} \exp \{ -y^2/2 \} dy$$

where the variable y is Gaussian with zero mean and unity standard deviation.

P_d , the probability of crossing the final threshold, is calculated by evaluating which sets of initial threshold crossings allow a final threshold crossing. For the given mode, $P_d = 4.533 \times 10^{-3}$.

The increase in the P_{fa} is calculated by estimating the number of detections per scan which could be expected from sidelobes. Assuming 100 fully correlating signals per scan and assuming four sidelobes with approximately this P_d (i.e., the peak sidelobe on each side has this P_d and then the second sidelobe on each side, which is at 9.75, has less than this P_d), the number of additional false alarms per scan is $N_{fa} = 400 \times 4.533 \times 10^{-3} = 1.81$. In the initial design, the number of false alarms was 2.66. The total number of false alarms is, therefore, increased to 4.47 per scan. This gives a new P_{fa} of 1.68×10^{-5} . From curves of P_d vs snr parameterized by P_{fa} , a snr loss of less than 0.1 dB is incurred for compensating for the increase in P_{fa} . Thus, an additional loss of 0.1 dB added to the previously designated loss of 0.9 dB gives a total of 1.0 dB.

¹ Hansen, V.G., "Optimization and Performance of Multilevel Quantization in Automatic Detectors," IEEE AES-10, No. 2, March 1974, pp 274-280.

The simplified analysis has shown that the sidelobes due to worst case Doppler offsets do not significantly affect the performance of the three-channel pulse compressor. The reduction in snr loss from 2.5 dB for the single channel pulse compressor to 1.0 dB for the three-channel pulse compressor shows the marked improvement in performance for the latter.

A key feature of the validation was to measure the response curves of the channels as a function of Doppler offset. In order to provide a coded input signal that simulated Doppler returns, the test setup shown in Figure 4-13 was employed. Offsetting the coherent oscillator simulates a Doppler return. Since the compressed pulsewidth using the system clocks was about 1/3 the SPUR required pulse width, the Doppler frequencies were adjusted accordingly. Thus the results presented must be scaled for the SPUR case.

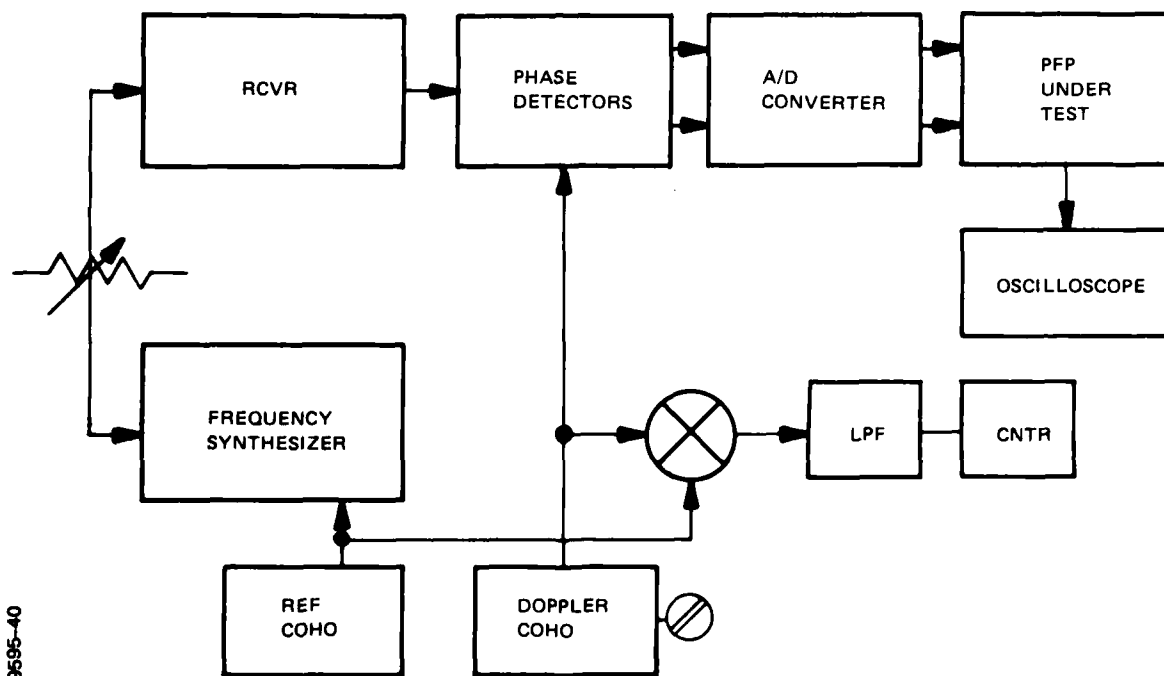


Figure 4-13. Simulated Doppler returns are obtained by using separate coherent and reference oscillators.

The theoretical response curves and measured data points for each channel as a function of Doppler frequency are shown in Figure 4-14. These measured points are the average response taken every 20 samples using a logic analyzer monitoring each channel before Greatest-of-Selection. Qualitatively, the channel responses are a good match to the theoretical curves of peak response. The video from each channel when the signal has a Doppler offset of -34.7 kHz is shown in Figure 4-15 (a-c). As can be seen, the response from the negative channel is maximum at the peak and the zero channel is reduced about 2 dB. The positive channel which should be down about 9 dB was very erratic. This behavior is attributed to feedthrough at the main bang time (a potential method for eliminating this coupling is to inject the code at IF, thereby gaining additional isolation from standard coaxial cables). The output of the GOS under the above conditions is shown in Figure 4-16.

The calculated reliability for the PFP based on the detailed design is 9.05 failures per 10^6 hours. This value is 1.66 failures per 10^6 hours higher than estimated during the SPUR Conceptual Design. The estimated power is 16 watts based on the measured 6 watts and an estimated 10 watts for the modified board made to the SPUR requirements. This is the same as the SPUR Phase I estimate.

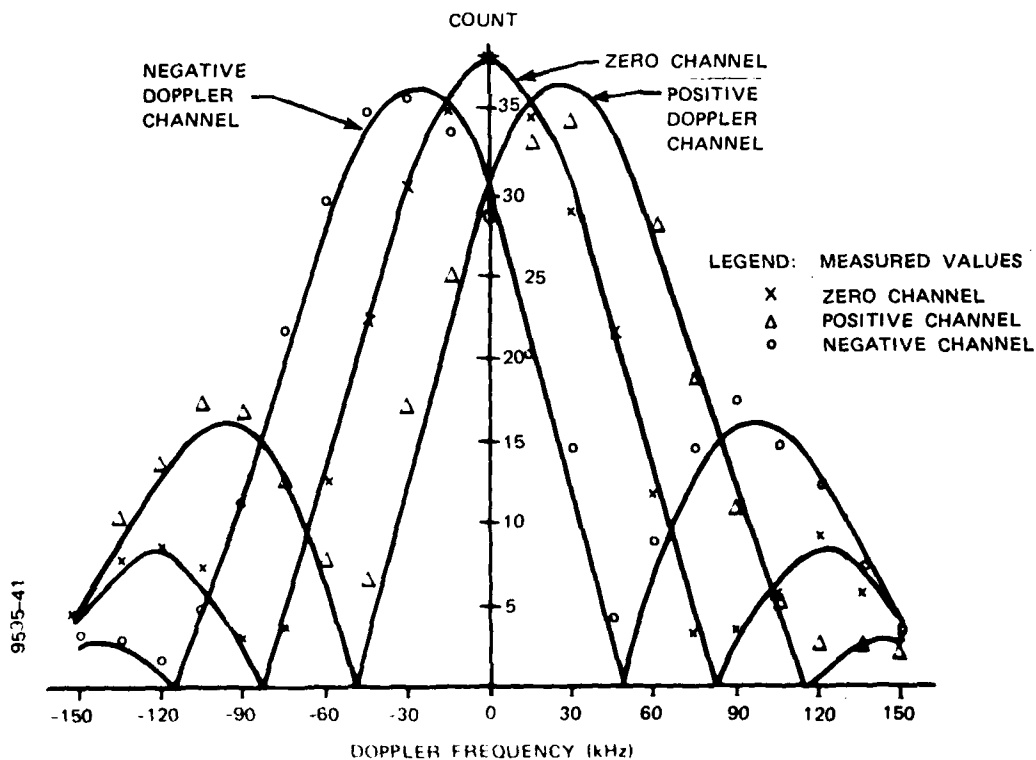
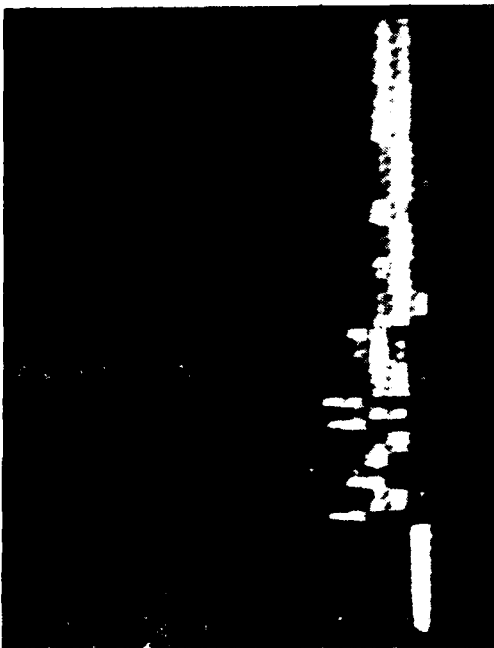
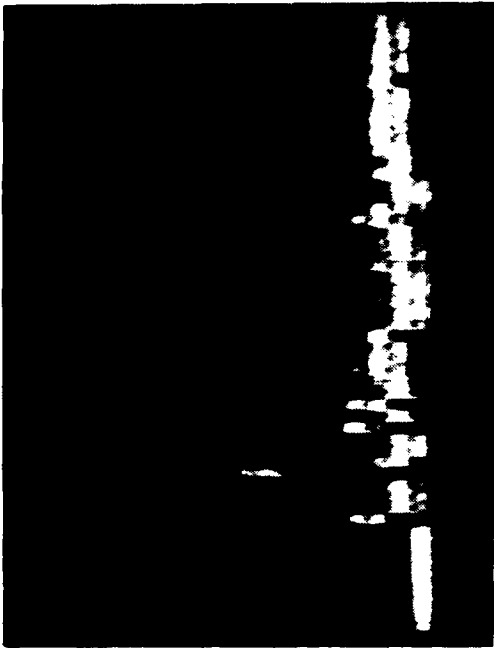


Figure 4-14. Measured values are plotted for each value in the theoretical curves.

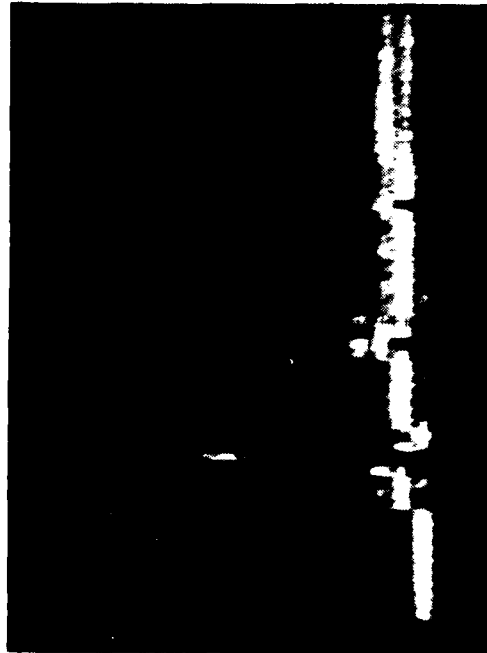


a) POSITIVE CHANNEL



b) ZERO CHANNEL

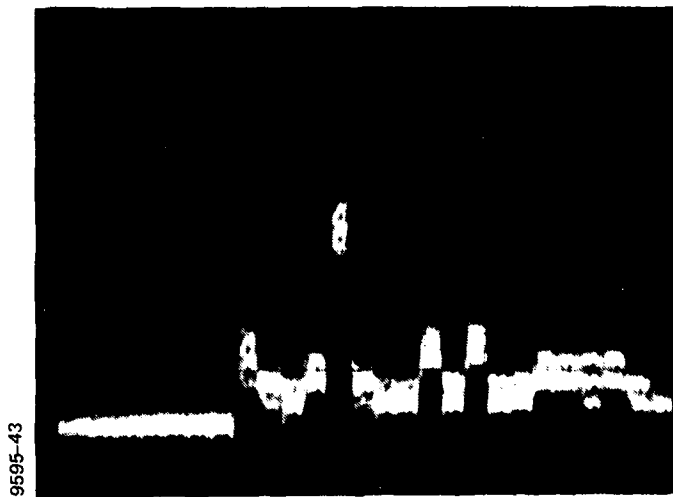
SCALE =
VERTICAL
0.5 v/div
HORIZONTAL
2 μ sec/div



c) NEGATIVE CHANNEL

9595-42

Figure 4-15. Compressed video from each channel to signal offset to -34.7 kHz.



SCALE =
 VERTICAL
 0.5 v/div
 HORIZONTAL
 1 μ sec/div

Figure 4-16. The output from the greatest-of-selector contains the worst case sidelobes of each channel.

4.3 POST-DETECTION PROCESSING FUNCTION

The Validation Program for the PDP Function was to develop the firmware program. One key requirement during this development was to minimize the interface hardware required by making maximum use of the RPM-II characteristics. This requirement leads to an alternate implementation from the Phase I recommended implementation. The new implementation is discussed below and contrasted to the previous one.

The Post-Detection Processing Function performs a sequential "greatest-of" operation across the Doppler filters followed by post-detection integration over about one radar beam-width (four hits). The integrated output is examined by detection logic which makes the decisions regarding target presence/absence for output to the data processor.

Two design alternatives were evaluated in detail during Phase I for use as the SPUR post-detection integrator: the binary and the multinomial detection methods. While both methods use a double threshold process, in the multinomial method the output of the first-threshold process is quantized to 2-bits as opposed to the single bit used in the binary case. When 2-bits are used in the first-threshold, signal-to-noise ratio loss in the post-detection integrator drops from 1.1 dB for the binary detection method to 0.4 dB for the multinomial detection method. Thus for the SPUR, a multinomial detector using two bits at the output of the first-threshold was used in the preliminary design effort.

The Post-Detection Integration (PDI) for the SPUR includes firmware for use in a RPM-II module and associated hardware interface. The Post-Detection Integration programs a) noncoherent video integration of four two bit values (one azimuth beamwidth), and b) automatic target detection on the integrated video. The PDI program receives the first-threshold data from the hardware interface and formats four of the two bit values as an eight bit address for a PROM, which performs the second-threshold. In the SPUR Phase I design, this second-thresholding was done by performing pattern recognition on the bits through a firmware routine. With the new implementation and more detailed design, the estimate for the instruction count has increased from the 155 instructions of Phase I to 200 instructions. The PDI program is shown in block diagram form in Figure 4-17 and is explained in further detail below.

The hardware necessary to interface with the PDI program and radar system is incorporated in an interface unit. This PDI interface unit (see Figure 4-18) takes the compressed video from the Post-Filtering Processor into a sequential (over the filters) "greatest-of" circuit where the data is compared to three thresholds and the result reduced to two bits. The two-bit quantized value is sent to the RPM-II through its input first-in, first-out (FIFO) memory port. The interface unit also contains the PROM used in the second-thresholding process. In the SPUR Phase I implementation, the PDI interface unit had buffer memory for input messages which would be unloaded by the PDI firmware after an interrupt. In the new interface unit, messages are sent to the RPM-II input FIFO as they occur. The PDI input routines store them into a buffer on the RPM. This change saves the additional buffer memory of the interface board. Another change in data handling

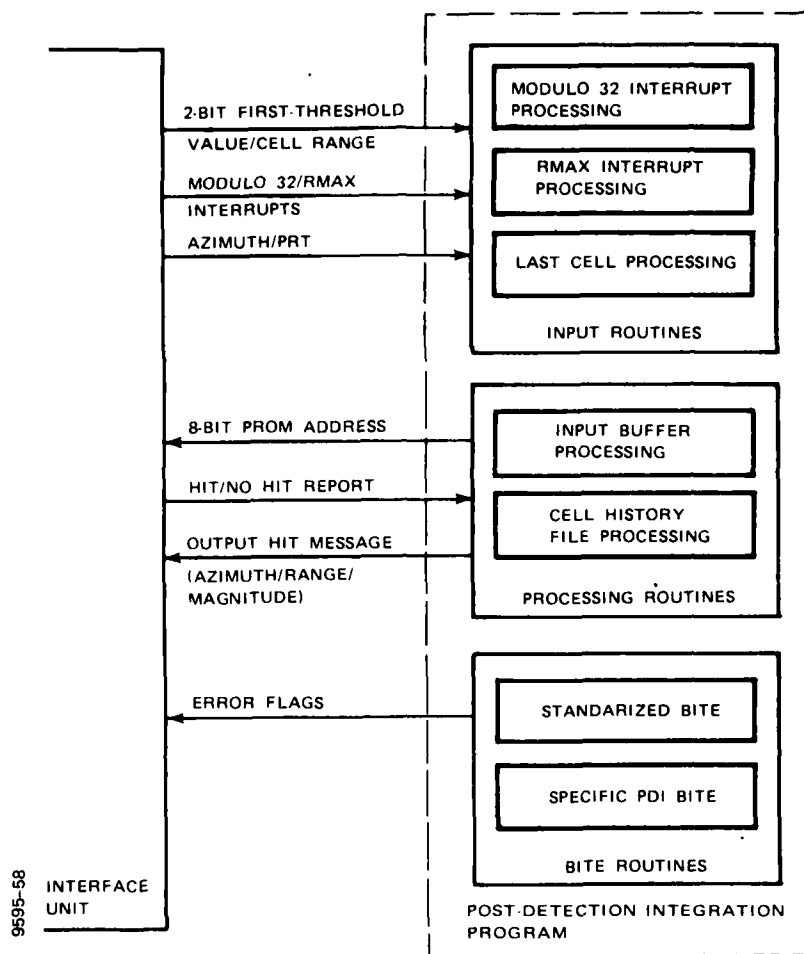


Figure 4-17. PDI program block diagram

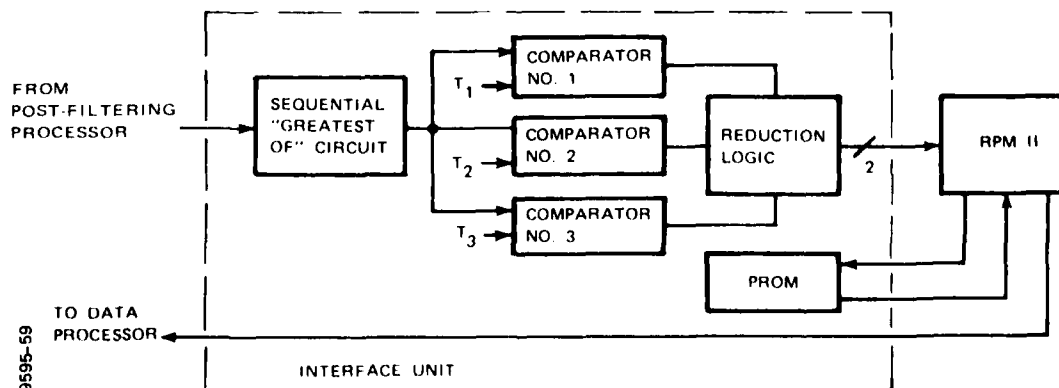


Figure 4-18. PDI interface unit

is recommended at the output. In Phase I, the output results from the PDI program went through an external shift register to the data processor. In the new interface unit the output messages consisting of three words are stored in buffer memory in the RPM-II and are unloaded through the RPM-II output FIFO to the data processor.

The PDI program has three basic parts: 1) Input Routines, 2) Processing Routines and, 3) BITE Routines. A Program Processing Requirement is provided in Appendix D. The input routines include Modulo 32 Interrupt Processing, RMAX Interrupt Processing and Last Cell Processing. The processing routines included Input Buffer Processing and Cell History File Processing. BITE Routines include system BITE and specific BITE for the PDI.

Input Routines

The hardware interface unit loads the RPM-II input FIFO with the two-bit quantized output of the first-threshold process as it occurs. With each two-bit first-threshold value the range is included in the sixteen-bit input word. The Modulo 32 Interrupt Processing is done when a modulo 32 interrupt is received indicating that the input FIFO has been loaded with 32 words out of the 64 available. The RMAX Interrupt Processing input routine reads the PRT and azimuth counters and records the radar azimuth in a table which is used to calculate the azimuth for that pulse transmission group. When the PRT Counter indicates the last pulse of a group, the remaining words in the input FIFO are stored into the buffer. The last word in each pulse transmission group is flagged before it is loaded into the input FIFO; when this flag is detected azimuth is calculated from the table of azimuths recorded every PRT. The azimuth is calculated by taking an average of the table and adding a pipeline delay factor.

Processing Routines

Program Control is then passed to the processing routines. The Input Buffer Processing performs the video integration over one azimuth beamwidth (four, first-threshold two bit values). This integration is performed by masking out the two bit value in the input word and storing it into a Cell History File in the least significant bits of an eight bit word to be made up of four successive first-threshold values. These eight bit words are stored in the Cell History File indexed by range. As the Cell History File is sequentially cycled through during the second-threshold process, each word is left-shifted two bits to make room for the next 2-bit first-threshold value for each range. The Cell History File Processing Routine sequentially reads the eight bit words from the Cell History File and outputs the eight bit word as a PROM address sent out by the RPM-II over an I/O bus to the second threshold PROM on the hardware interface unit. Stored in the PROM at that address is hit/no hit report which indicates whether or not a target hit has occurred. For each hit report a message is formatted and stored in buffer to be later sent to the data processor through the interface unit. This message is three words and contains range, azimuth and magnitude information. The range information tells at what range the target hit has occurred and the azimuth information is the azimuth calculated as an average from the radar azimuth values recorded each PRT plus the pipeline delay factor. The magnitude information provided is the eight bits that had been used as the PROM address.

BITE Routines

The BITE routines provide fault-monitoring and isolation for the RPM-II and PDI firmware. The BITE function schedules and executes RPM-II Diagnostic Routines (local standardized BITE) and system test target. The BITE routines also include specific test cases for the PDI firmware and the RPM-II hardware specifically used during the post-detection integration process. These are in the form of regular BITE to determine error conditions and Extended BITE (EBITE) to check error conditions. Output from the BITE routines are error flags to indicate failures in hardware or firmware.

The hardware interface to the PDI firmware program provides for input messages to the PDI, interrupts to the PDI, radar parameter counters readable by the PDI, the PROM used by the PDI in the second-thresholding process and a path for the output messages from the PDI to the data processor.

The input message from the interface unit is one word and contains the two-bit quantized value from the first-threshold process. This input message also contains the range of that cell and a flag to indicate the last range cell for a pulse transmission group. This message is loaded into the PDI RPM-II input FIFO as it occurs. Three interrupts are input to the PDI RPM-II through the interrupt register. They are the Power-Up Interrupt, Modulo 32 interrupt, and the RMAX interrupt. The Power-Up interrupt indicates a power-up condition and has highest priority. The modulo 32 interrupt indicates that the RPM-II input FIFO has been loaded to the half full condition and has priority over the RMAX interrupt. The RMAX interrupt flags every RMAX time in a pulse transmission group.

Two counters are read by the PDI firmware during PDI program operation. These counters are the PRT counter and the azimuth counter. They allow the PDI firmware to reset for new groupings and to calculate the azimuth of each integrated group.

The PDI program and interface hardware has been configured to minimize external hardware, while still maintaining realtime operation using less than half of the available time. The above described implementation achieves these goals.

4.4 THE STATE PROCESSOR

4.4.1 STATE Processor Concept

The Status, Transformation and Test Evaluation (STATE) Processor provides a means for centralized control of a distributed BITE system. The STATE Processor collects and reports the status of the entire Signal Processor to the systems' digital processor. It monitors and commands all modules or units in the Signal Processor to perform specific BITE tests and return the results to the STATE Processor when requested. The units perform their BITE tests asynchronous to the STATE Processor and hold the results of the test until they are taken by the STATE Processor. The STATE Processor also has the ability to reconfigure any of the redundant modules in the Signal Processor in the event of a failure detection except for the A/D converters. A redundant unit can be enabled and switched-in to replace the faulty unit.

Since the STATE Processor has total control over redundant unit switching in the SPUR Processor, the STATE Processor must in itself be a highly reliable unit. The design goal for the reliability of the STATE Processor is specified at 4.0 failures per 10^6 hours. One method of design used to achieve a highly reliable unit, as required by the STATE Processor, is to employ Triple Modular Redundancy (TMR). Three separate processors, each operating from its own program and data memory, perform identical operations. The resulting data is then voted on and taken as the majority value. Also, to add to the STATE Processor reliability, the design must be able to fit on the standard 14 by 15 inch, 210 IC (16-pin) board.

4.4.2 STATE Processor Architecture

The STATE Processor is designed using TMR design concepts to increase the reliability of the unit. In a TMR design, some amount of the hardware is triplicated and the output data voted on to produce the correct result if one of the three replicated units fails. The outputs of the voting circuits are then used by each of the three units. Serial data transfers and parallel to serial converters within each of the three processors can also be TMR to further enhance the reliability.

An architecture for the STATE Processor based on TMR techniques is depicted in Figure 4-19. It consists of three microprocessors, each having its own ROM and RAM, executing in synchronism and in parallel. Each of the microprocessors executes an identical microprogram stored in their respective triplicated ROMS. The data to each of the processors is identical and is stored in the processor's corresponding RAM. The voting is performed on the data output from the memory with triplicated voting circuits. Each voter receives data from the three memories, votes on the data, and provides the result to its respective microprocessor. This method of operation protects both data and instructions read from the memory as well as providing additional protection for hardware memory addressing failures and microprocessor program counter failures. The three processors are reset with each coherent group trigger to synchronize the microprocessors.

Data out of the microprocessors are output to a parallel I/O port, one for each of the three redundant processors. The parallel data is then transferred to a 16-bit parallel to serial converter and shifted out serially. Each of the three processor's parallel to serial converter

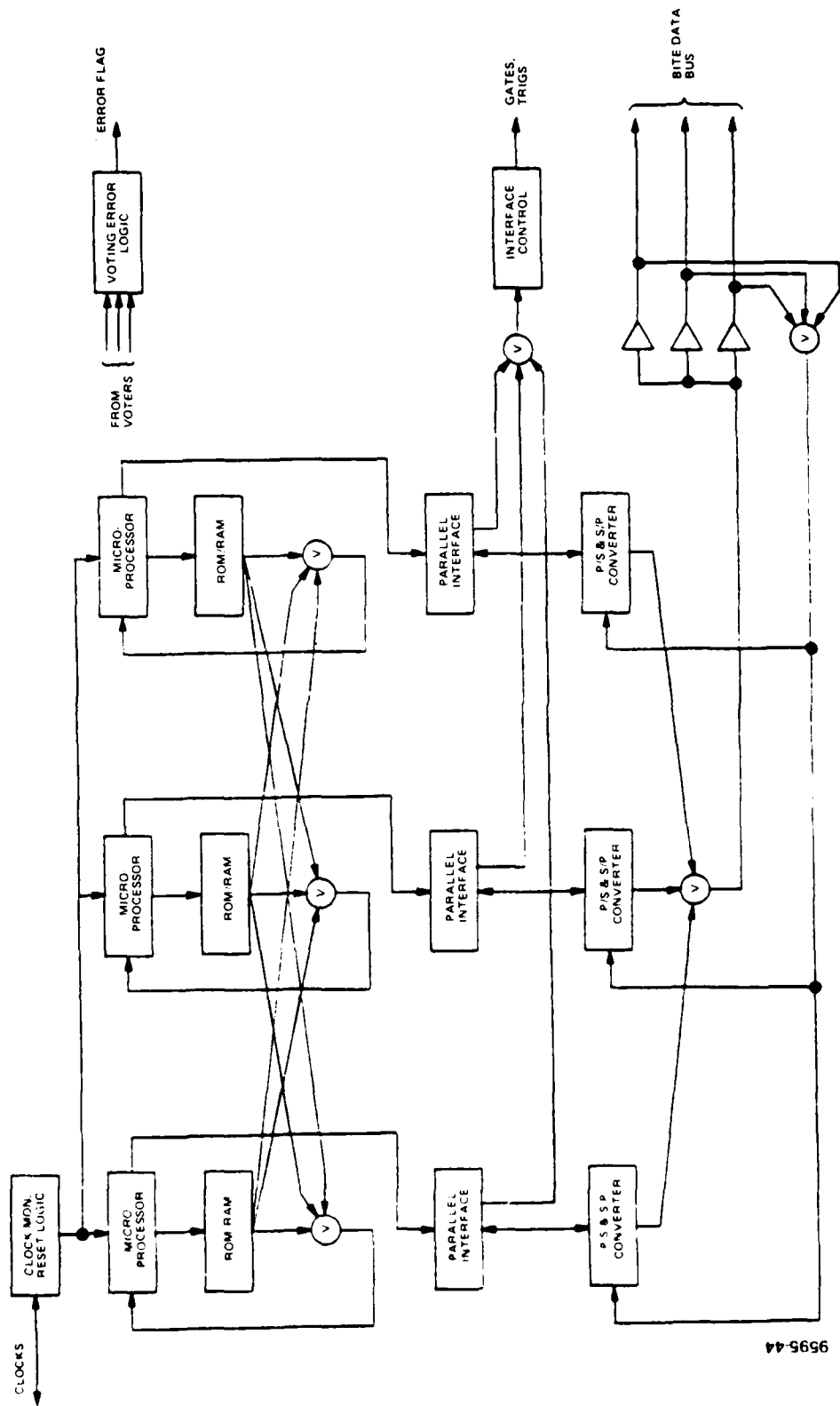


Figure 4-19. STATE Processor Block Diagram Showing Triple Modular Redundancy

serial output data lines are used as input to another voting circuit. This voter checks the operation of the microprocessors' parallel I/O ports and the parallel to serial converter. The output of the voting circuit is 1-bit of serial data which drives the BITE interface. Serial data received from the BITE interface is distributed to each of the three processors' serial to parallel converters which produces a parallel 16-bit word at the termination of the input transfer. This parallel data is transferred to the microprocessor through the parallel I/O port.

The STATE Processor interfaces to each of the other units in the Signal Processor to send commands, test data, control information and to receive unit status and test result data. The STATE Processor interfaces to the A/D Converters, Doppler Filter Modules (DFM), Post Filtering Processor, Power Control Unit, Data Processor, Interface Board, and RPMs. These interfaces are illustrated in Figure 4-20, and a summary table of the types of data to be transferred is provided in Table 4-V. The data transfers between the STATE Processor and the other units are accomplished through the use of a common bidirectional serial BITE data bus. The parallel to serial converters interface to the bus through the voting circuit and three-state bus drivers to form a TMR serial bus configuration. The data received from the three serial BITE data bus lines are voted on and distributed to the three processors' serial to parallel converters for input to the microprocessors.

Control of the BITE data bus is handled by the STATE Processor. The control signals consist of two shift enable gates to each unit in the Signal Processor, one for shifting data into the Processor from the selected unit, the other for shifting data out of the STATE Processor to the selected unit. The shift gates are sixteen clocks in duration to enable 16-bit word transfers. A maximum of sixteen units can be interfaced to the STATE Processor in this scheme. Figure 4-21 illustrates the interface between the STATE Processor and the other units in the Signal Processor.

The basis for this STATE Processor architecture is to achieve a high reliability design capable of uninterrupted operation without operator action. The Triple Modular Redundant (TMR) design philosophy is used because of its relatively simple implementation compared to spare processor methods with automatic error detection and switching mechanisms. The voter circuits are placed only at the memory outputs and serial data outputs to reduce the number of voting circuits required in the processor. The following two sections describe the implementation of the STATE Processor using two microprocessor families, the Zilog Z80A 8-bit microprocessor and the Motorola 68000 16-bit microprocessor.

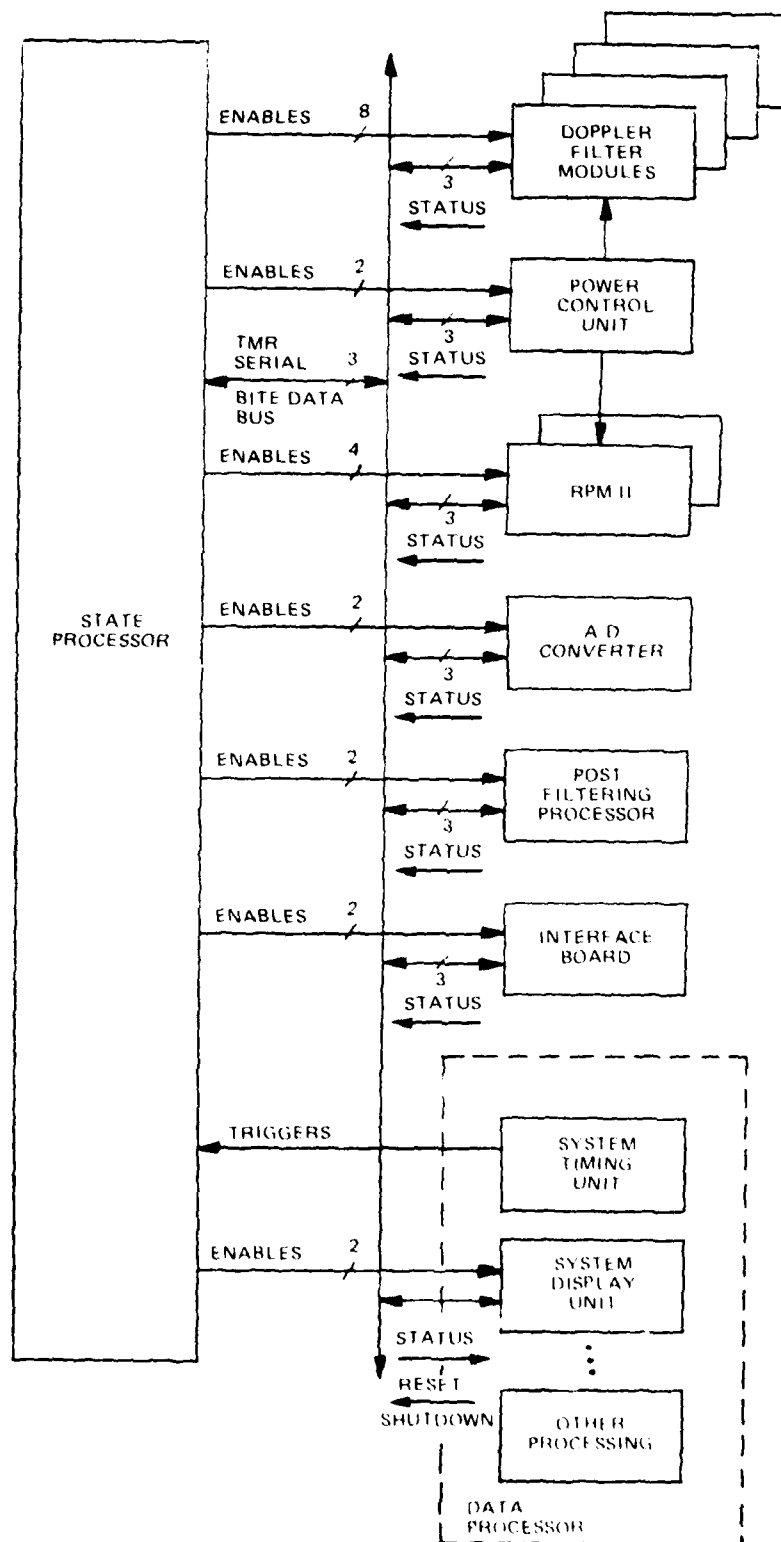
4.4.3 Z80A Based STATE Processor Design

A STATE Processor design based on the Zilog Z80A family of microprocessor components is illustrated in Figure 4-22. The block diagram shows the Z80A CPU used as the TMR microprocessor. Associated with each processor are separate program ROM storage and scratchpad RAM. The outputs of the ROM and RAM are three-state and are enabled onto the voter inputs, which are implemented with PROMs. The outputs of each processor memory are compared with the outputs from the other two processors and is taken to be the majority vote and used as input to each Z80A CPU. Since both instructions and data pass through these voters any errors in instructions, data, program counter address, and memory address are covered by the redundancy.

TABLE 4-V. Data Transfer Between State Processor and Other Spur Modules

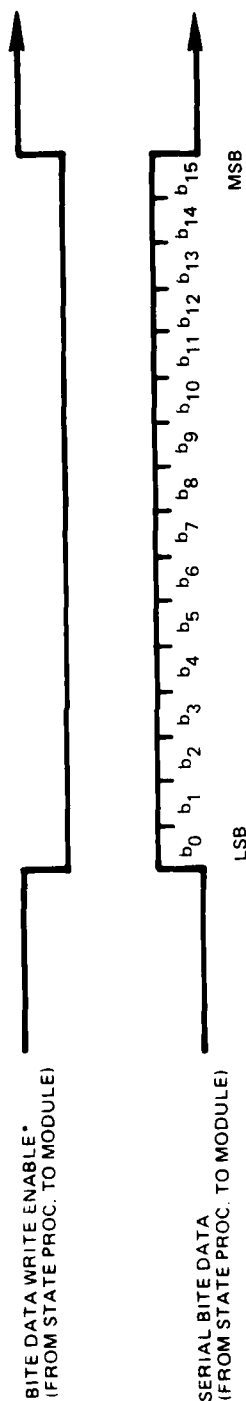
<u>Module</u>	<u>Data</u>	
	<u>To STATE Processor</u>	<u>From STATE Processor</u>
A/D Converter	Active Channels Status of Standby Channel	BITE Read Enable Test Target Request BITE Test and Reset BITE Write Enable
Doppler Filter	BITE Results I Filter Data (16 Bits) Q Filter Data (16 Bits) Extended BITE Results I Filter Data (16 Bits) Q Filter Data (16 Bits) Parity Results on Input Data Checksum Results on Output Data	Filter Number Assignment and Extended BITE BITE Data (24 Bits) BITE Read Enable BITE Write Enable
Post-Filtering Processor	BITE Results Channels Status	Filter Select Control BITE Read Enable BITE Write Enable
Interface Board	Detection of Double Error in Clutter Map Status of Clutter Map Modules BITE Results Clutter Map Interface Logic PDI Interface Logic	Memory Modules Active Control BITE Read Enable BITE Write Enable Degraded Modes Control Zero Channel Disable
Radar Processing Module (RPM-II)	BITE Results Processor Routine I/O Checks Extended BITE Results	RPM-II Selection Extended BITE Requests BITE Read Enable BITE Write Enable

The inputs and outputs from the Z80A CPU to the parallel/serial and serial/parallel converters are handled by the Z80A PIO parallel interface port. Each Z80A CPU has its own set of PIOs as illustrated in Figure 4-22. A detailed design of the serial interface logic for one of the three microprocessors is provided in Figure 4-23. Three PIO chips, one for a 16-bit input port, the second for a 16-bit output port, and the last for control and triggers comprise the total interface to the Z80A CPU. The remaining circuitry of Figure 4-23 constitutes the parallel/serial, serial/parallel converter. A 4-bit counter is used to generate a 16-clock wide shift gate for either input or output operations.

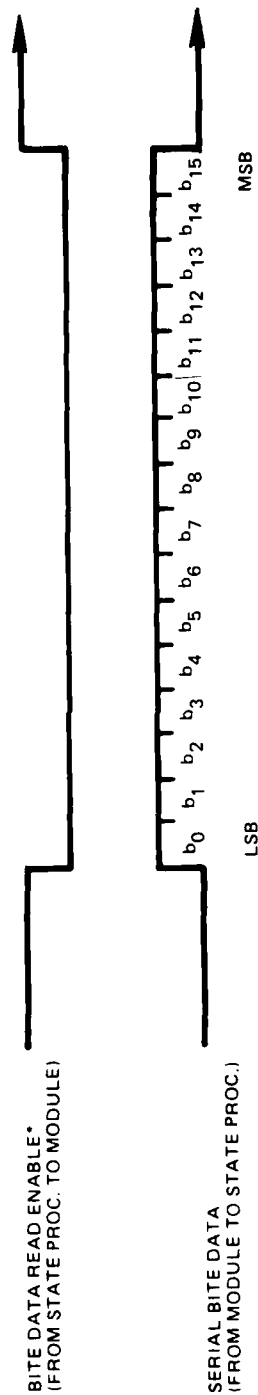


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Figure 4-20. STATE Processor Interface Diagram



STATE PROCESSOR TO SPUR MODULE DATA TRANSFER



SPUR MODULE TO STATE PROCESSOR DATA TRANSFER

Figure 4-21. STATE Processor serial BITE data interface protocol

9595 47

The serial data produced by the parallel/serial converter in each of the three processors is voted on, which protects the PIO and parallel/serial converters from single component failures, and output in parallel to three bus drivers which drive the TMR BITE data bus. The data received as input by the STATE Processor from the three bus lines are voted on and applied in parallel to the serial inputs of each serial/parallel converter. Figure 4-24 illustrates the necessary logic to accomplish this function. Also depicted in the same figure is the unit select logic which determines the unit that receives the shift in or shift out gate. A 4-bit unit address and two select bits are output from the control PIO that causes one of sixteen output lines to become active and initiate the shift operation.

An estimate of the board chip count required to implement this Z80A microprocessor design is summarized in Table 4-VI. This number represents the equivalent number of 16-pin chip locations occupied by the design. The standard 14 inch X 15 inch board can accommodate 210 16-pin chips.

The table also shows that the design, using 180 16-pin equivalent chips, can be constructed on one board. Also contained in Table 4-VI is the calculated TMR reliability of the STATE Processor, $\lambda = 2.88$. The design goal was set at $\lambda = 4.0$ and the Z80A STATE Processor design meets this goal.

A summary of the general features of the Z80A based STATE Processor design is provided in Table 4-VII. Included in this table are microprocessor word and memory size, speed and instruction execution times, reliability, and power consumption. The main advantages of the Z80A design are the wide commercial acceptance of the Z80A microprocessors, availability of software support for the microcode, numerous development systems available, and smaller package size.

4.4.4 68000 Based STATE Processor Design

An alternative design of the STATE Processor uses the Motorola 68000 16-bit microprocessor as the basis for the TMR processor. This design is illustrated in block diagram form in Figure 4-25. The 68000 also has triplicated program ROM and RAM memories associated with it. The outputs from both the ROM and RAM are three-state and are enabled into the voters, implemented with PROMs, for error correction. The output of the voter is used by the 68000 as input data. The method of voting on the memory output is identical to that described in the Z80A design except the memory words are now 16-bits wide instead of 8-bits. Again, the redundancy will mask any single processor error in instructions, data, program counter address, and memory address.

Input and output data transfers from the 68000 CPU to the parallel/serial and serial/parallel converters is accomplished using the Motorola PIA Peripheral Interface Adapter. This peripheral chip, designed for use with the 68000 8-bit microprocessor family, is usable with the 68000 CPU. Data transfers between the 68000 and the PIA are all 8-bits at a time.

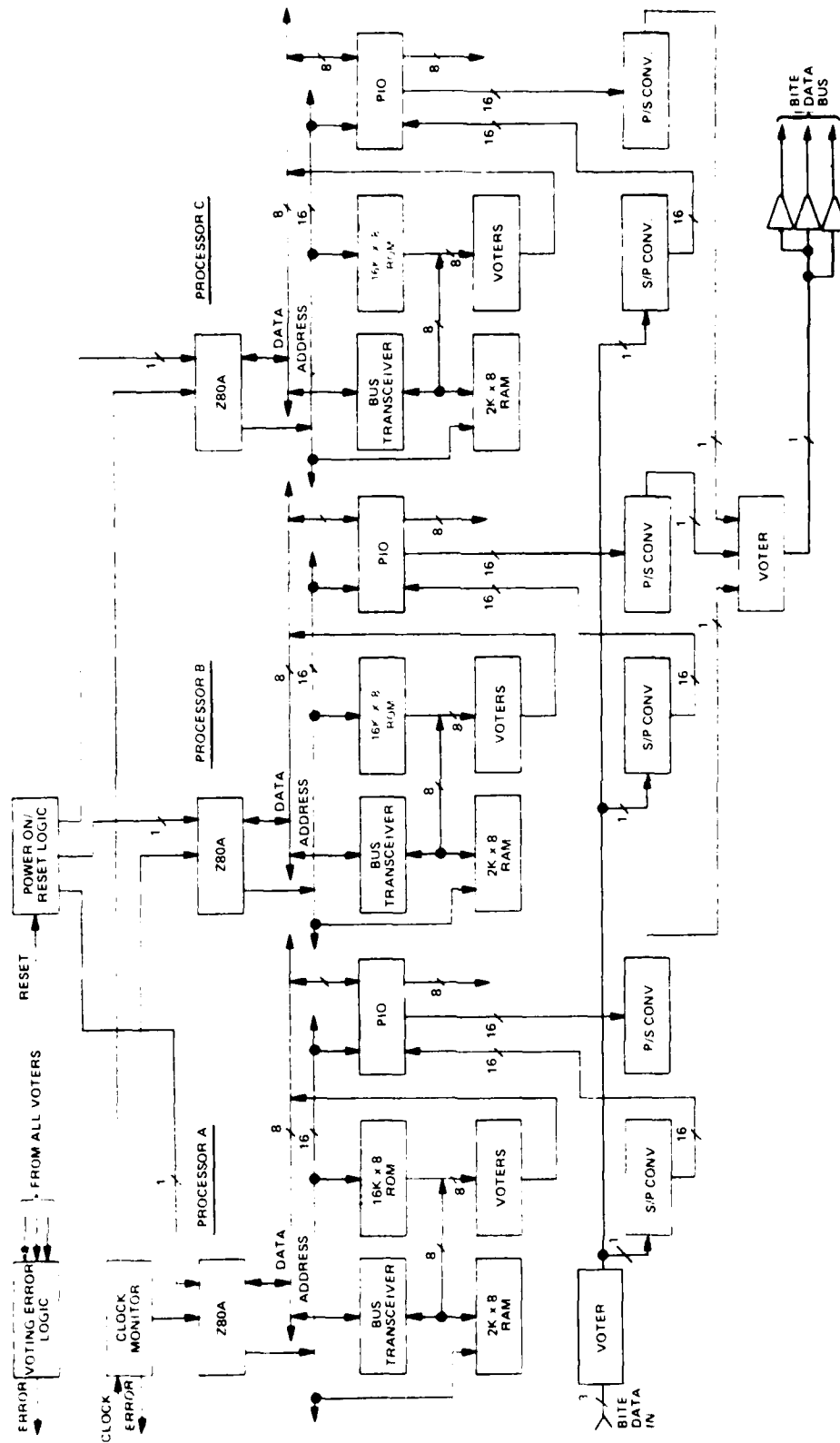


Figure 4-22. Z80A STATE Processor Block Diagram

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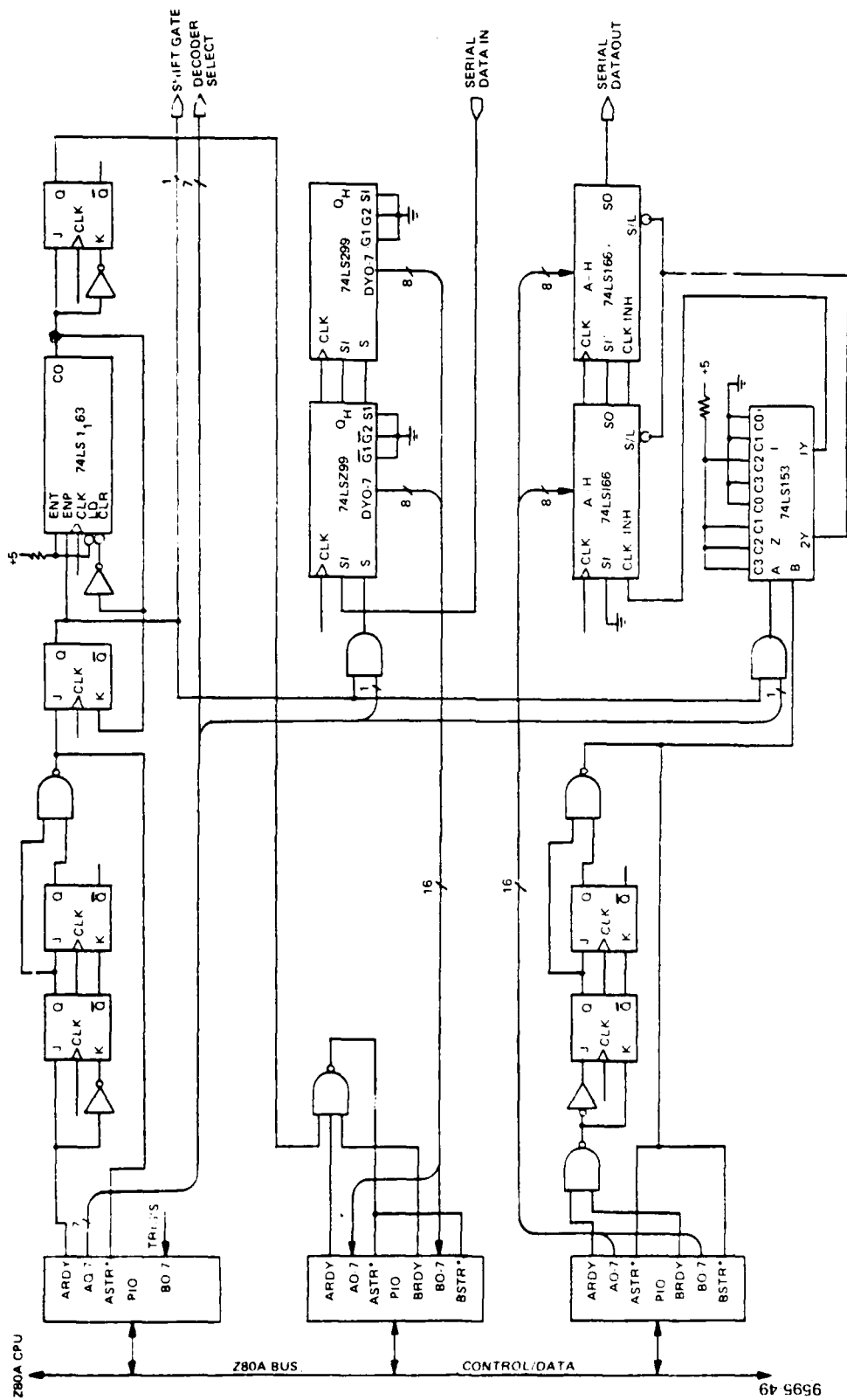


Figure 4-23. 780A STATE Processor BITE Serial Interface Logic

Table 4-VI. Z80A STATE Processor Chip Count

IC Type	Quantity	No. Pins	16-pin equiv.	λ
Z80A CPU	3	40		4.78
Z80A PIO	9	40	54	1.35
2K X 8 RAM (2K X 8)	3	24	9	3.464
Bus Transceivers 74LS245	3	20	4	0.034
16K X 8 ROM 8 (2K X 8)	24	24	54	0.896
Voters (IM5623 PROM)	12	16	12	0.039
JK F/F 74LS109	10	16	10	0.033
P/S Conv. 74LS166	6	16	6	0.070
S/P Conv. 74LS299	6	20	8	0.094
Dual 2:1 MUX 74LS153	3	16	3	0.033
4-Bit Counter 74LS163	3	16	3	0.071
1:8 Decoder 74LS138	4	16	4	0.033
SSI Gates	13	14	13	0.058
Total Chips	99		180	

Reliability

$\lambda_{\text{Single Proc.}}$	=	20.376
λ_{TMR}	=	2.54
λ_{Serial}	=	0.340
λ_{Total}	=	$\lambda_{\text{TMR}} + \lambda_{\text{Serial}} = 2.54 + 0.340$
λ_{Total}	=	2.880

Table 4-VII. STATE Processor Characteristics

	Z80A	MC68000
Data Word Size	8 bits	16-bits (32-bits internal)
Max. Instruction Length	3 bytes	3 words
Add Instruction Time	1 μsec (8-bit)	1 μsec (16-bit)
Clock Frequency	4 MHz	8 MHz
ROM Size (per CPU)	16K X 8-bits	8K X 16 bits
RAM Size (per CPU)	2K X 8-bits	2K X 16 bits
CPU Package Size	40 pin	64 pin
Power Requirements	33.16 W	41.71 W
Failure Rate, λ (per 10^6 hours)	2.88	4.94

However, since processor speed is not a prime requisite for the STATE Processor, this interface will suffice. Figure 4-25 illustrates the interfacing of the PIA to the processor. The detailed logic for the PIA and parallel/serial, serial/parallel converters for one of the three processors is illustrated in Figure 4-26. Two PIA chips are used to interface to the special purpose logic. One is used as an 8-bit input/output port to send data to the parallel/serial converter and receive data from the serial/parallel converter. The other PIA is used to output command bits to control the operation of the parallel/serial interface and to receive timing trigger information. A 4-bit counter is used to generate a 16-clock wide shift enable gate for 16-bit serial data transfers between the STATE Processor and other units.

The PIAs and parallel/serial converters are protected from single failures with voters on the outputs of the three parallel/serial converters. The serial output of the voter circuit is buffered through three bus drivers onto the TMR BITE data bus. Input data received by the STATE Processor from the BITE data bus is voted on and used as input to the serial/parallel converter in the same manner as the Z80A design (refer to Figure 4-27). The unit selection logic which controls the unit that receives the BITE enable shift gates is shown in the same diagram. A 4-bit unit address and two select bits are output from the control PIA is used to enable one of the sixteen input or output shift enable lines. This is likewise similar to the Z80A design.

A reduction in the number of PIA chips compared with the Z80A design is necessary to accommodate the entire design on one board. One PIA from each processor is removed leaving an 8-bit input port and an 8-bit output port, instead of 16-bit. It is also necessary to reduce the ROM size to fit the design on one board. The ROM is 8K X 16 bits (16K X 8 bits for the Z80A). An estimate of the board chip count using the 6800 microprocessor is summarized in Table 4-VIII. This number represents the equivalent number of 16-pin chip locations occupied by the design. The standard 14 X 15 inch board can accommodate 210 16-pin chips. The number of 16-pin equivalent chips, 201, used in this design meets the goal of having the STATE Processor on a single board. Also included in Table 4-VIII are the results of the reliability calculations. The goal established was to have a failure rate of $\lambda = 4.0$. The actual design calculations produce a $\lambda = 4.940$ for the STATE Processor. In these calculations it was assumed that the MC68000 has a $\lambda = 10.0$ since the calculated value using the model produced an unrealistic result. The 68000 has the equivalent of 38000 transistors. A 65K RAM has a $\lambda = 8.5$ but contains a greater number of equivalent transistors. Hence the value 10 was selected as reasonable for use in comparative calculations.

Table 4-VII (Section 4.4.3) is a summary of the general features of the 68000 microprocessor based STATE Processor design. Included in this table are microprocessor word and memory size, speed and instruction execution times, reliability, and power consumption. The advantages of using the Motorola 68000 microprocessor in the STATE Processor design are that it is a 16-bit processor enabling easier arithmetic manipulation of 16-bit data and it is a new and powerful state-of-the-art microprocessor.

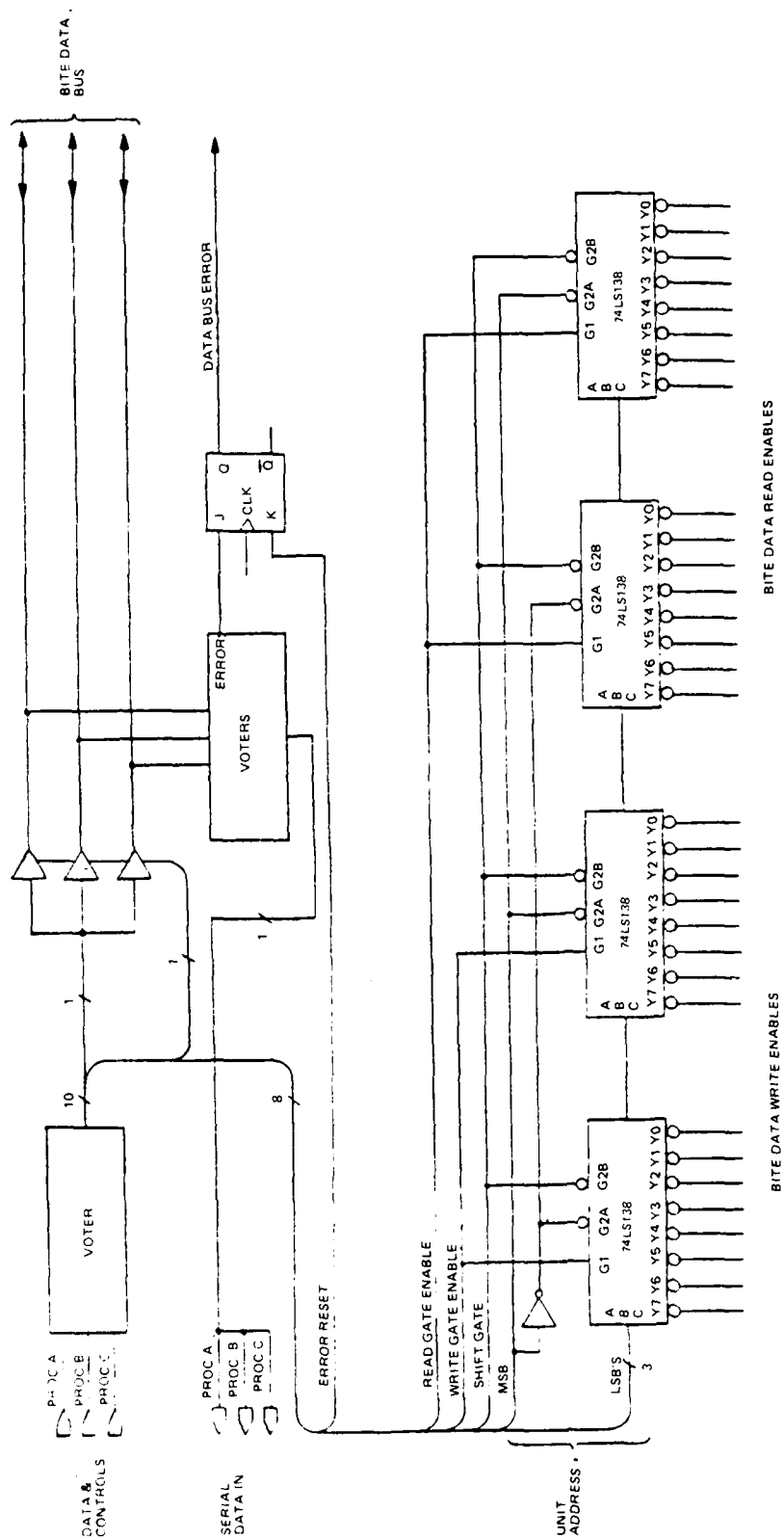


Figure 4-24. Z80A State Processor BITE Interface Control Logic

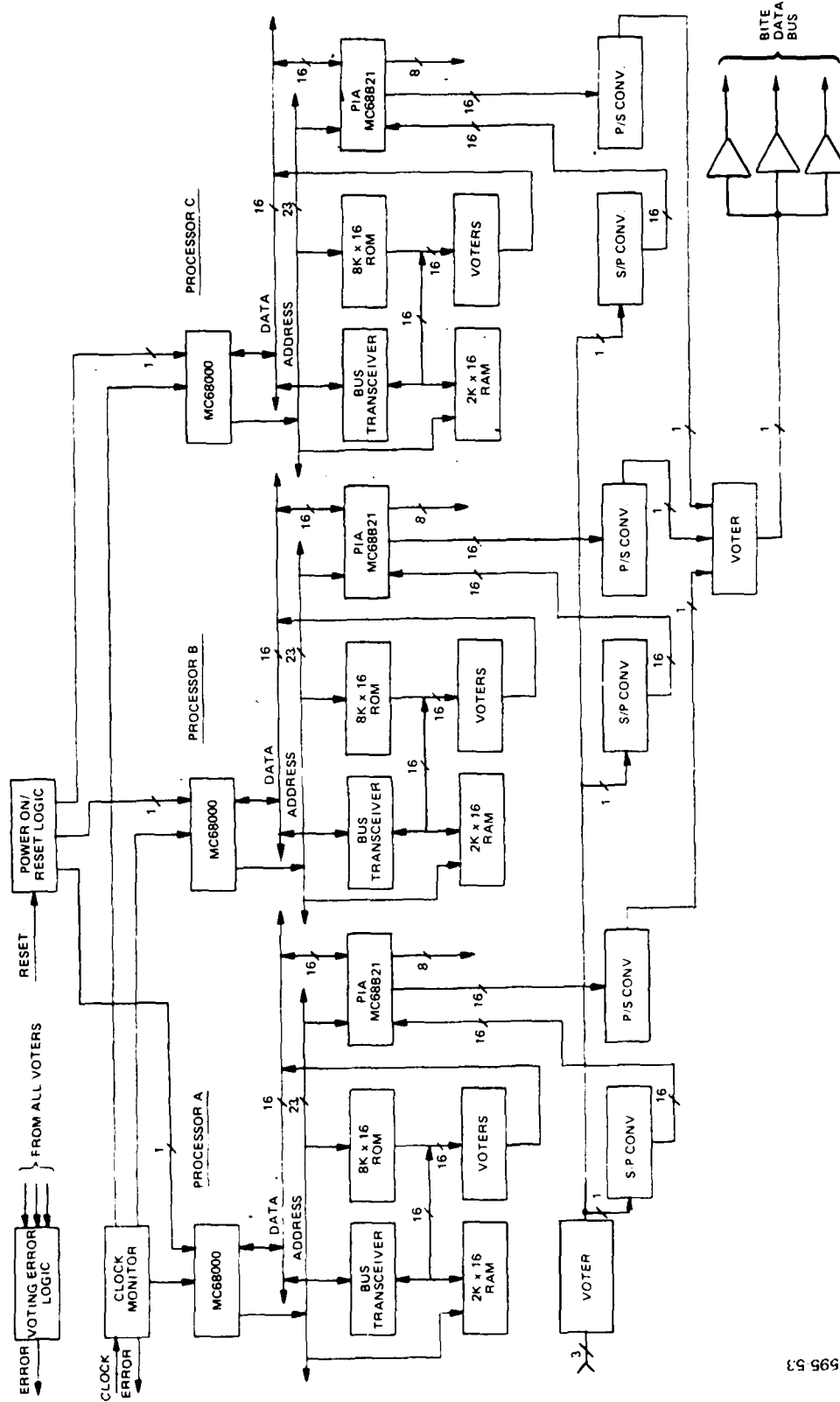


Figure 4-25. MC68000 STATE Processor Block Diagram

Table 4-VIII. 68000 STATE Processor Chip Count

<u>IC Type</u>	<u>Quantity</u>	<u>No. Pins</u>	<u>16-pin equiv.</u>	<u>λ</u>
68000 CPU	3	64	24	7093*
68B21 PIA	6	40	27	1.35
2K X 16 RAM 2 (2K X 8)	6	24	15	3.464
Bus Transceivers 74LS245	6	20	9	0.034
8K X 16 ROM 8 (2K X 8)	24	24	54	0.896
Voters (IM5623 PROM)	21	16	21	0.029
JK F/F 74LS109	7	16	7	0.033
P/S Conv. 74LS166	6	16	6	0.070
S/P Conv. 74LS299	6	20	9	0.094
Dual 2:1 MUX 74LS153	6	16	6	0.033
4-bit Counter 74LS163	3	16	3	0.071
1:8 Decoder 74LS138	4	16	4	0.033
Dual 2:4 Decoder 74LS139	3	16	3	0.034
SSI Gates	13	14	13	0.058
Total Chips	114		201	

Reliability

$$\lambda_{\text{Single Proc.}} = 27.895$$

$$\lambda_{\text{TMR}} = 4.60$$

$$\lambda_{\text{Serial}} = 0.340$$

$$\lambda_{\text{Total}} = \lambda_{\text{TMR}} + \lambda_{\text{Serial}} = 4.60 + 0.340$$

$$\lambda_{\text{Total}} = 4.940$$

***Note:** The model used to calculate the failure rate of the 68000 produces an unrealistically high value for the LSI device. A $\lambda = 10$ is assumed for further calculations of reliability. This value is supported by the fact that a 65K RAM contains more transistors than the 68000 (38000 transistors) and has a $\lambda = 8.5$.

4.4.5 STATE Processor Firmware Functions

The STATE Processor firmware program performs eight functions as follows:

- a) Initialization and Self-Check (ISC)
- b) BITE Data Evaluation (BDE)
- c) Extended BITE Evaluation (EBE)

- d) Reconfiguration
- e) SPUR Status Communication (SSC)
- f) BITE and Redundancy Evaluation (BRE)
- g) Degraded Modes Configuration (DMC)
- h) Orderly SPUR Shutdown (OSS).

A flow diagram for the STATE Processor firmware functions is illustrated in Figure 4-28. The Initialization and Self-Check (ISC) function is initiated by a power-on or external reset command. This function shall verify that the STATE Processor is capable of operating in a sane manner. If a failure is detected, the SPUR Status Communication (SSC) function is notified to provide a "no-go" status to the system and the Orderly SPUR Shutdown (OSS) function is invoked. A watchdog timer is used by the system to monitor the STATE Processor outputs and will cause an external reset to be sent to the STATE Processor in the event of communications failure. A second consecutive timeout will cause an Orderly SPUR Shutdown to occur. Following successful initialization and self-check, the ISC function defines an initial system by energizing the pre-defined Doppler Filter Modules and RPM II units. At this point normal SPUR operations begin and the BITE Data Evaluation (BDE) function is invoked.

The BDE supplies the necessary BITE signals to interrogate each module or unit to output the results of performing a BITE operation. The BITE results are evaluated and if deemed to be correct, the next module in the sequence is interrogated. If, however, a BITE test for a module has failed, the Extended BITE Evaluation (EBE) function is invoked. After all of the modules have been queried and no faults detected, the SPUR status is updated and the BITE and Redundancy Evaluation (BRE) function is called.

The EBE function requests Extended BITE (EBITE) to be run on the questionable module and the results are evaluated. If examination of the results of the extended BITE tests yields correct results, control is returned to the BDE function for a retest and a transient failure is suspected. A second failure of the same BITE will cause the Reconfiguration function to be invoked. The Reconfiguration function is also called if the EBITE indicates a failure.

The Reconfiguration function will make an attempt to recover the Signal Processor system using selective redundancies. If a redundant module exists in the area of the indicated failure the Reconfiguration function deactivates the faulty module and activates the spare replacement module. A set of configuration commands will initiate operation of the new module. The SPUR status is updated via the SSC function and control is returned to the BDE function. If no redundant module exists for the failed module, the Degraded Modes Configuration (DMC) function is invoked.

The SPUR Status Communication (SSC) function periodically communicates the status of all SPUR modules to the system. It also evaluates the new status and makes a decision to invoke the Orderly SPUR Shutdown (OSS) function if necessary. The status communications to the system is used to reset the watchdog timer and must occur at a periodic time interval. The SSC function is normally invoked by the BITE and Redundancy

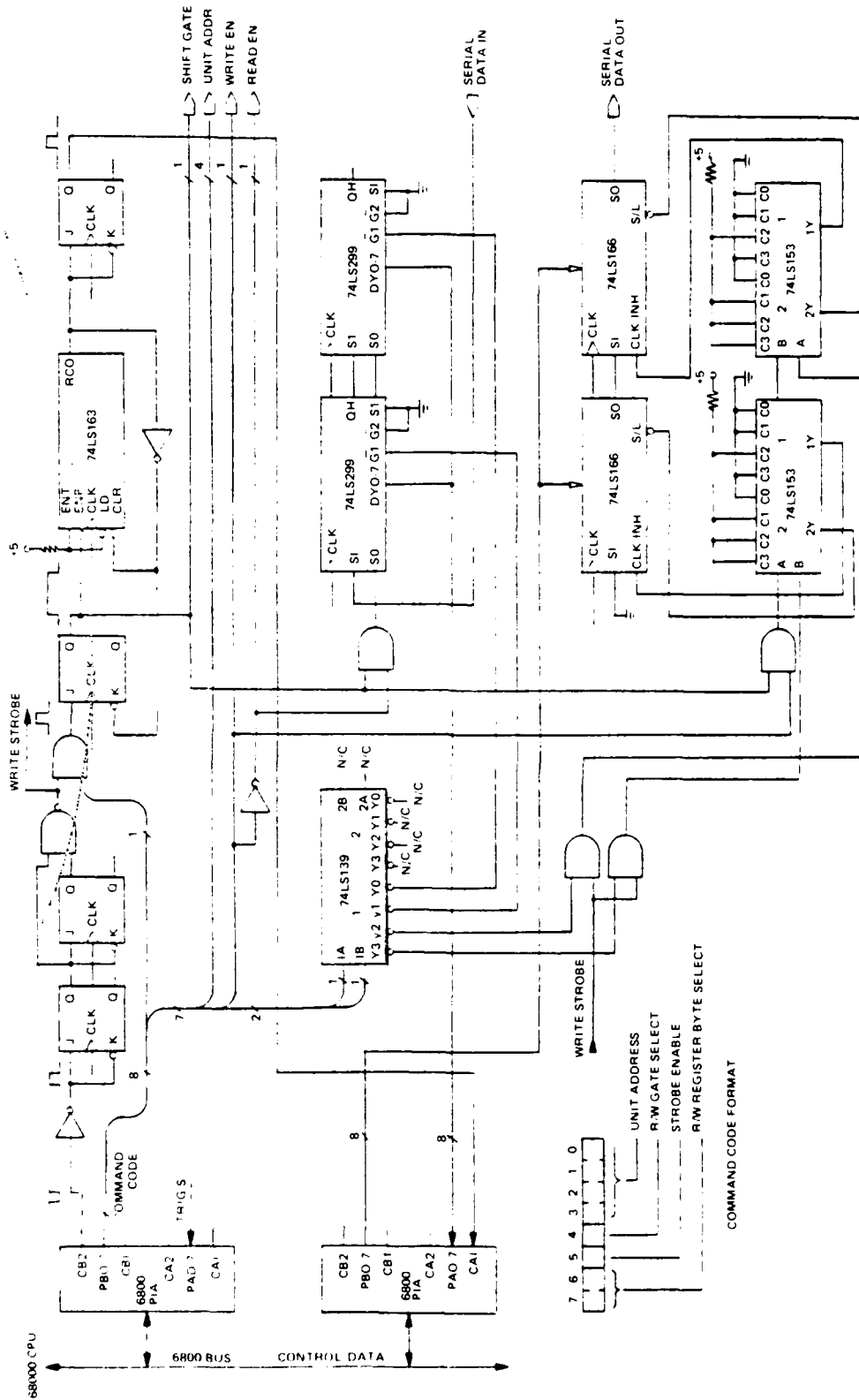


Figure 4-26. MC 68000 STATE Processor BITE Serial Interface Logic

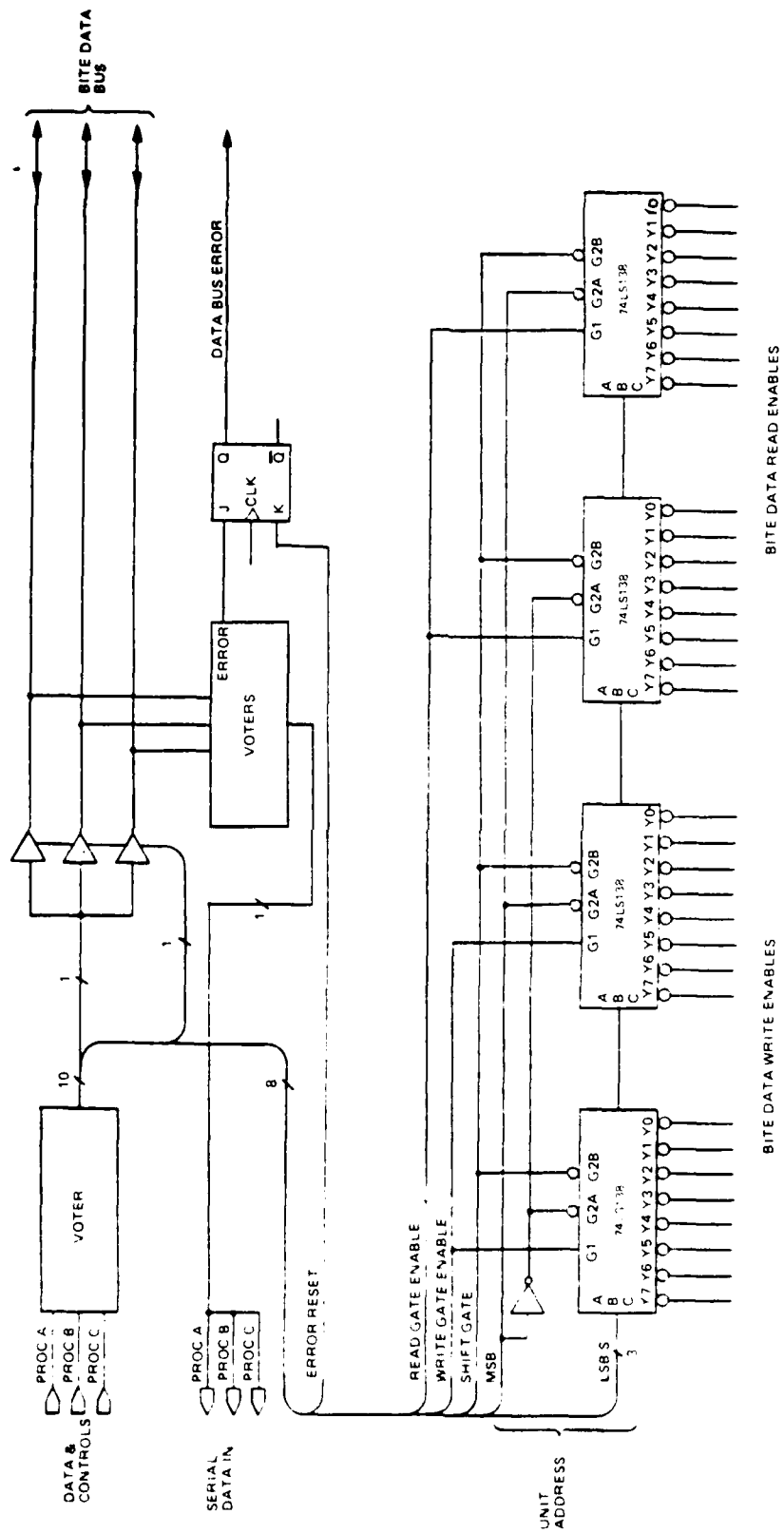


Figure 4-27. MC 68000 STATE Processor BITE interface control logic

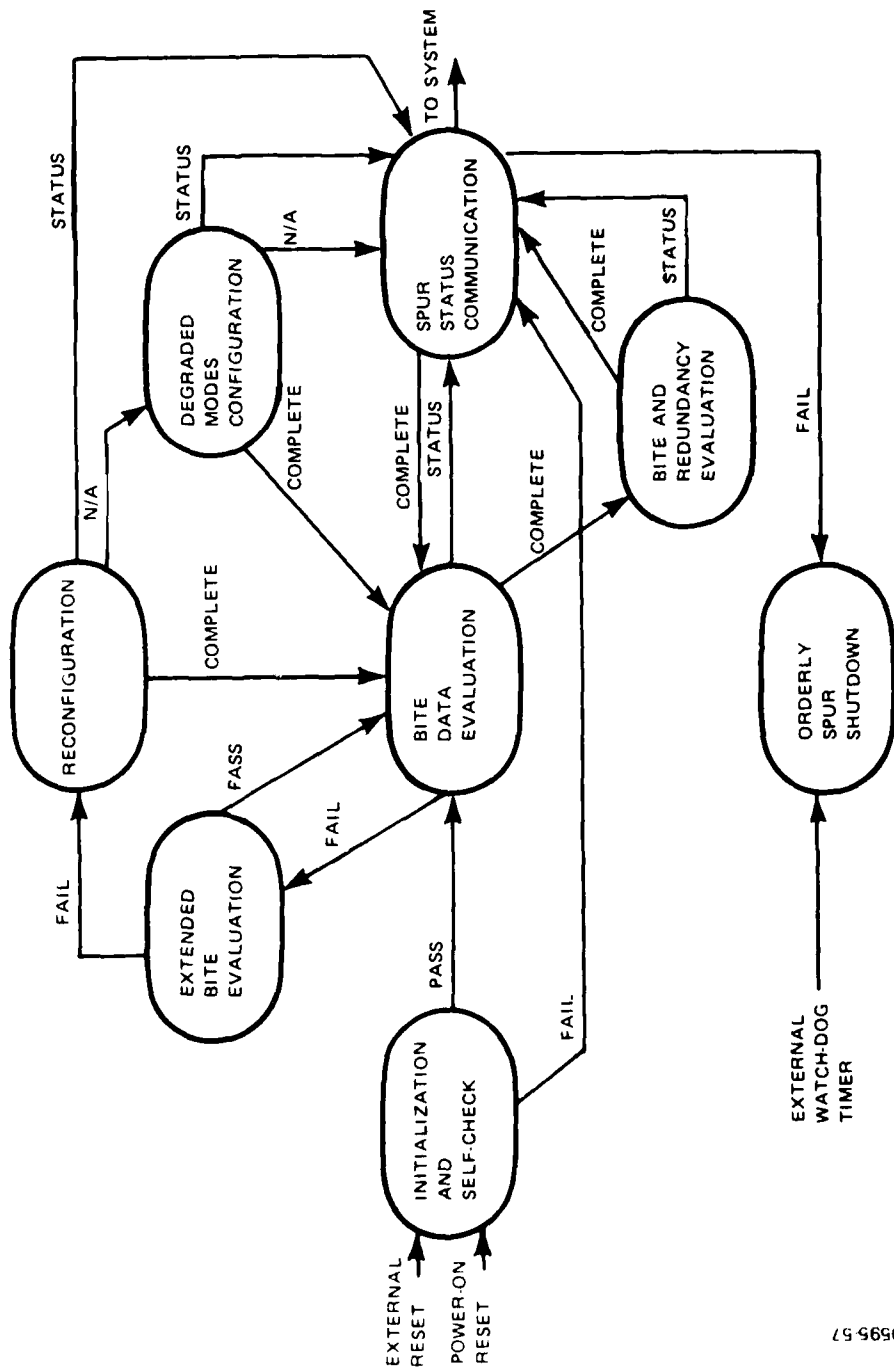


Figure 4-28. State processor flow diagram

Evaluation (BRE) function after the status is checked. On completion of Status Communication, control is returned to the BDE function. Two special cases occur if the ISC function detects a failure or the DMC Function has been called with no degraded modes of operation for the failed condition. These two instances request status communication to the system and invoke the OSS function.

The Degraded Modes Configuration (DMC) function is responsible for activating pre-defined degraded modes of operation when normal SPUR operation is impossible. An example of a typical degraded mode of operation is to excise the zero filter when the clutter map is deemed inoperative. The DMC function provides status to the SSC function and returns control to the BDE function. If no degraded mode exists for the identified failure, the DMC function invokes the SSC function.

The BITE and Redundancy Evaluation (BRE) function supplies BITE data to each SPUR module to verify the operation of the module BITE and selective redundancy. A typical procedure to perform this test is to supply BITE data which causes an error to be found when the results of the BITE are evaluated. The detection of the error will force a reconfiguration to occur and activate the spare module. The spare module is then tested using the normal BITE then reset back to spare status on completion. The SSC function is then called. The BRE tests are conducted twice daily based on a comparison of Azimuth North pulse counters.

The Orderly SPUR Shutdown (OSS) function is invoked to shutdown the SPUR Processor when it has an unrecoverable failure. This prevents invalid data from being transmitted to the system. This function is called by the SSC function following the evaluation and transmission of the SPUR status to the system. The OSS function can also be activated by the system via interrupt when the watchdog timer has timed out two consecutive intervals.

Section 5

RECOMMENDATIONS

The SPUR Phase II Validation Program was designed to verify critical circuits recommended for the Optimum Processor during the SPUR Phase I Conceptual Design. During the five-month effort, this verification was begun by designing and fabricating one major subsystem of the processor (the Post-Filtering Processor), designing another major subsystem (Doppler Filter Modules), designing an example of a calibration loop (A/D Zero Stabilization Loop), and performing the conceptual design for two additional units (STATE Processor and PDI Firmware). These designs and tests have helped to verify some aspects of the recommended optimum SPUR, but the detailed tests to validate functional performance and the fault-tolerant aspects of the design could not be accomplished.

A simple recommendation, therefore, would be to complete the program and perform the requisite tests. However, a more pragmatic recommendation is to evaluate what can be gained from these tests given that the potential applications have been delayed and that the technology is moving ahead very rapidly. Thus the real key to the following recommendations is the question: to what extent is the optimum SPUR subject to major technology advances?

Probably the two areas most subject to technology advances are the A/D converter and the pulse compressor. The SPUR Validation Program recommended paper design of an eleven-bit A/D converter, and design, fabrication, and testing of a calibration loop. Certainly the eleven-bit converter design, though based on current state-of-the-art componentry, could be eclipsed by technology, thereby allowing twelve-bit units to be a better development recommendation. On the other hand, the calibration loop is relatively insensitive to the technology and to the number of bits in the converter for verifying its functional characteristics. Therefore a reasonable recommendation is to develop and prove the calibration loop concept around an existing A/D converter.

The pulse compression system depends on a novel mechanization to provide improved performance at reasonable increase in cost. It is judged likely to remain the method of choice in the near future because its nearest competitor, a SAW line with linear CFAR, will depend on digital technology increases for improvement. Digital technology increases would then be applicable to the hardlimited binary phase-coded pulse compression also. In addition, the pulse compressor is insensitive to the number of bits in the converter since it operates on hardlimited data (I and Q sign bits). A second recommendation is to run definitive tests on the fabricated pulse compression system to verify the estimated performance.

The Doppler Filter Modules (DFMs), which implement Near-Optimum Filters, are not considered technology sensitive because they implement any general FIR filter

based on eight coefficients and have the capability to be expanded to operate on twelve-bit input data. Functional performance can be verified for reasonably expected technology changes. Therefore, completion and testing of the Doppler Filter Modules is recommended.

The concept of the STATE Processor is also relatively insensitive to technology, because the main items for verification are the control of the redundant elements of the processor and the internal reliability of the STATE Processor. In any case, a program-mable technology is recommended and since the STATE Processor is a dedicated unit, it is not judged to be speed critical. Two implementations were configured during Phase II using microprocessors with significant technology differences. The architecture of the STATE Processor in each case is the same. Therefore, the key verification task is to validate that the Triple Modular Redundancy (TMR) configuration works in the presence of faults and that external faults can be diagnosed and corrected. The first item is a hardware verification task dependent on the voter concept, not on the microprocessors, while the second is a firmware task dependent on the program and once again not the microprocessor. Since the STATE Processor verifications are microprocessor (and hence technology) independent, the STATE Processor is recommended for development and integration with the DFMs for internal and external fault recovery demonstrations.

The other portions of the SPUR Phase II Validation Program are only recommended at a lower level because of lesser risk reduction for the development dollar. However, the clutter map cell size is a reasonable item for further verification since its operation is a relatively empirical process.

Appendix A

PRELIMINARY PHASE II TEST PLAN

This Appendix describes the test plan that has been developed for use during the twelve month Phase II of the SPUR contract. Objectives of this plan are to verify the essential characteristics of the unattended radar signal processor identified during Phase I of the SPUR effort. These characteristics include the following:

- a) Functional performance,
- b) Power consumption.
- c) Reliability.
- d) Performance monitoring/fault isolation.
- e) Stability.

The test program described herein has been structured to demonstrate the above characteristics in a cost-effective manner. In particular, maximum use is made of available equipment and components. Moreover, emphasis has been placed on verifying the basic principles of high-performance and high-reliability designs, with less attention given to the specific devices themselves. In particular, there are no plans for reliability testing at the component level.

A.1 TEST PROCEDURES

The procedures to be followed in verifying the critical SPUR areas are discussed below. Selection of the specific procedure for testing a particular unit is determined by trading off the cost of the test including unit fabrication versus the potential benefits in reducing the risks.

- a) **Analysis** -- Analysis, will be conducted during Phase II with two principle objectives -- to verify the design requirements established for the processor units and to insure that the units and processor as a whole will satisfy the requirements of the SOW. Much of the analysis has been completed in Phase I; however, some analysis will be carried out in more detail in Phase II, and it will incorporate any changes that result during this phase.

In the reliability area especially, there will be a great deal of reliance on analysis for reliability predictions. Overall processor reliability will be determined by analysis.

- b) **Unit Level Tests** – Testing at the unit level shall be used in verifying the characteristics peculiar to each unit. Included in this category of tests are parameters such as speed, power, intraunit fault detection, etc. Internal reconfiguration or automatic calibration will also be demonstrated for units designed with these capabilities.
- c) **Processor Level Tests** – These tests will be conducted on the integrated processor hardware. The interfaces between processor units will be verified at this level as part of the processor integration. In addition, tests shall be run to verify the fault detection properties of the processor and to demonstrate the interunit reconfiguration operations. Furthermore, status monitoring and message reporting will be verified.
- d) **System Level Tests** – Tests at the system level will be conducted using the L-band test bed facility at ITT Gilfillan. These tests shall be used to determine the basic functional performance of the processor in an actual severe clutter environment. In addition, these tests shall be used to verify the functional requirements developed by analysis for the various units within the processor.

A.2 DETAILED TEST DESCRIPTION

The generic block diagram of Figure A-1 illustrates the five basic functions which comprise the SPUR. This functional breakout is sufficiently general to permit optimization of the individual functions, and, at the same time, is specific enough to support the identification and design of the processor units within each function.

The principle activity of Phase I was to determine the optimum configuration of the processor. In terms of the generic block diagram of Figure A-1, this required identifying the specific operations associated with each function and, simultaneously, the most effective implementation approach for each operation. Figure A-2 illustrates, at the unit level, the processor recommended as a result of the Phase I effort.

The major units of the processor are described below, along with the original general validation procedures for each. Specifications for the units have been developed, and these are included in the unit descriptions. Verification worksheets are also provided for each unit. The major characteristics of each unit are listed on these sheets, and associated with each applicable characteristic, is the requirement for that unit. These requirements are generally derived from the higher level processor requirements and in many cases are more appropriately classified as design goals.

During the detailed design process of Phase II, all requirements will be continuously addressed and reallocations will be established as necessary.

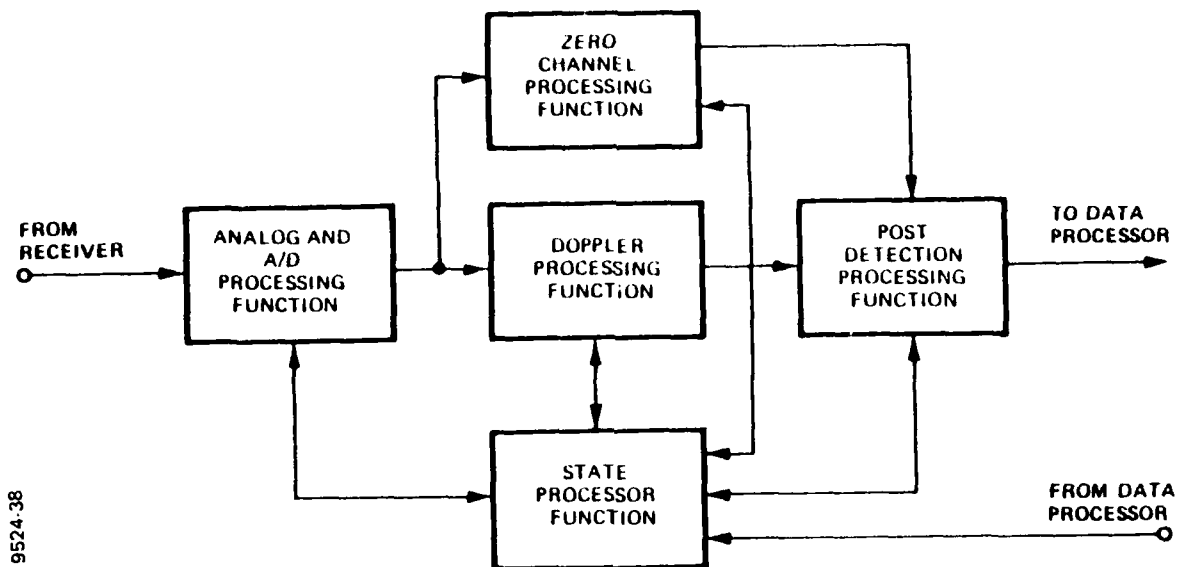


Figure A-1. SPUR generic block diagram depicting processing functions.

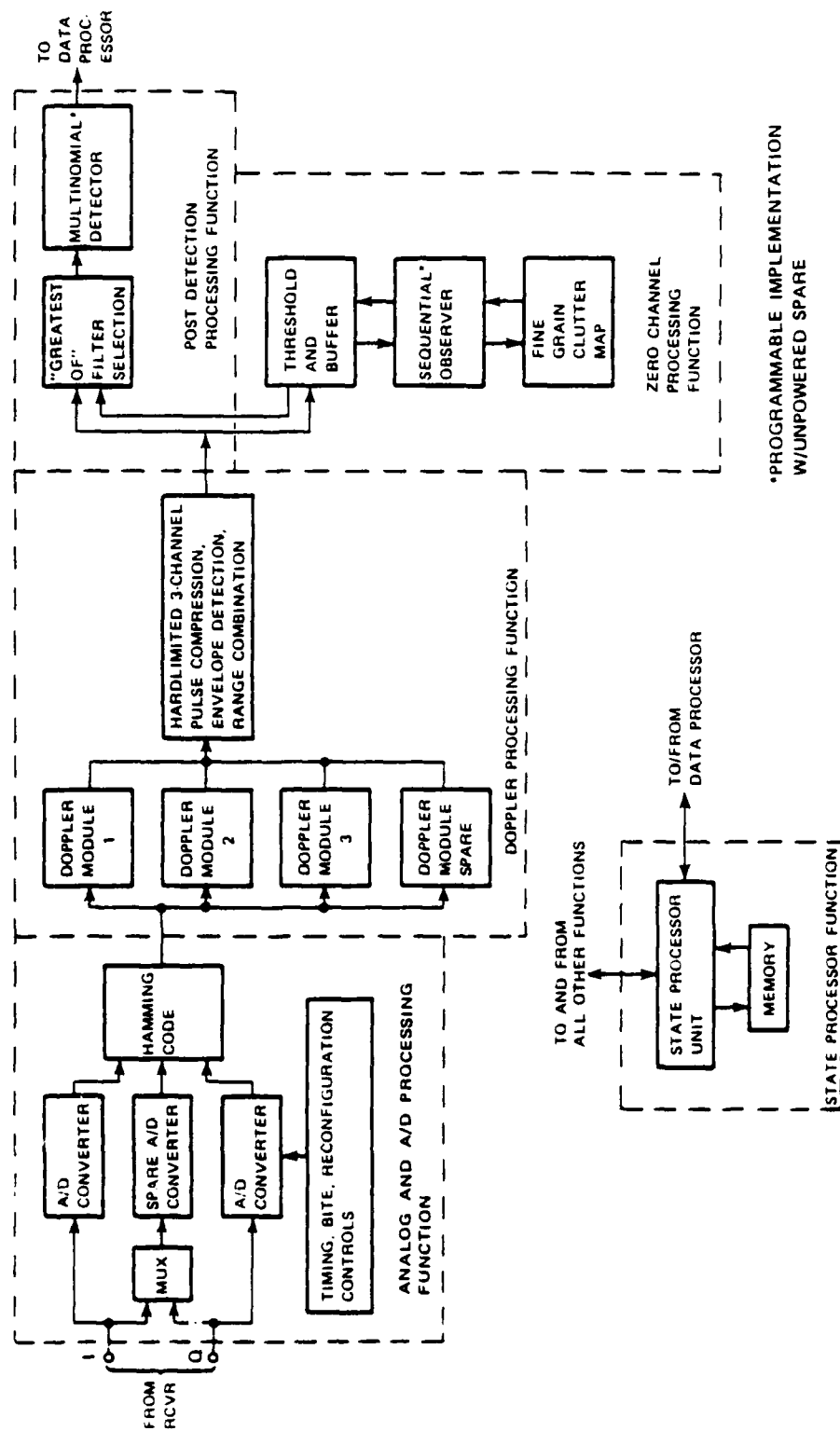


Figure A-2. Unit level SPUR block diagram for recommended processor

A.2.1 A/D Converter

For the processor under consideration, the A/D converter is considered a critical item. The dynamic range, sampling stability, and speed must be sufficient to satisfy the overall system requirements of clutter rejection, range bin size, and processing losses. Furthermore, the presence of analog signals and circuitry imposes the requirement for automatic calibration techniques to account for long- and short-term drift problems. Also, the converter reliability, fault detection and reconfiguration capabilities are important considerations and should be verified.

Table A-1 is a set of preliminary specifications for the A/D converter. These have been developed based on the total system requirements and are considered reasonable for use in an unattended radar. (Note: The gain and absolute linearity requirements are less critical than the differential linearity, feedthrough, and crosstalk requirements since the application requires relative and not absolute values.)

Unfortunately development of an A/D converter with all of these capabilities is expensive and would seriously limit the resources available for the rest of the verification plan. Consequently, we propose to verify the A/D converter through the following procedure:

- a) Design and develop an example of automatic calibration circuitry;
- b) Test calibration circuitry with commercial A/D;
- c) Implement system level tests with high-speed commercial, or in-house developed, A/D;
- d) Conduct preliminary design of two-step flash A/D converter unit;
- e) Develop power, reliability, cost, environmental factors, and special handling characteristics from the preliminary design and developed hardware.

The verification worksheet for the A/D converter is given in Table A-II.

A.2.2 Doppler Module

The Doppler module is also considered to be a critical item in the SPUR concept. We propose to design, develop, and test two of these modules during Phase II.

Table A-III provides a list of major performance specifications for the Doppler module, and the verification worksheet of Table A-IV identifies the validation procedures to be followed for the various parameters.

Table A-I. Analog/Digital Converter Specifications

Speed	0.618 μ sec maximum conversion time (Both I& Q)
Dynamic Range (Resolution)	11 bits
Power Consumption	38 watts
Losses	0.35 dB Quantization 0.8 dB Range Straddle (double sampling)
Calibration	dc Offset Control Loop
Reliability	9.14 f/10 ⁶ hours
Reconfiguration	2 converters with 1 hot standby
Modularity	1 board for complete unit
Environmental	0° – 120°F Operating; -70° – 100°F Storage
Interfaces	Receiver/Doppler Modules/STATE
Linearity	$\pm 1\%$
Differential Linearity*	± 1 LSB
Gain	$\pm 1\%$
Feedthrough	$\pm \frac{1}{2}$ LSB
Crosstalk	$\pm \frac{1}{2}$ LSB

*Monotonic over required temperature range. No missing codes.

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Table A-II. Verification Worksheet for A/D Converter

Characteristic	Requirement	Verification Approach				Remarks
		Analysis	Unit Level Demo	Processor Level Demo	System Level Demo	
Speed	0.618 μ sec Conversion Time (Both I & O)	X			X	Commercial or In-House A/D
Dynamic Range	11-Bits	X	X		X	Commercial or In-House A/D
Memory Size						
Power	38 Watts	X	X			
Losses	0.35 dB Quantization 0.8 dB Range Straddle	X			X	Commercial or In-House A/D
Program Instructions	N/A					
BITE/Calibration	dc Offset Control Loop	X	X			
Reliability	9.14 $\times 10^6$ hr	X				MIL-HDBK-217B,C
Reconfiguration	2 of 3 Required	X				
Modularity	1 board	X				
Environmental	0° - 120° F Operating -70° - 100° F Storage	X	X			
Special Handling	None	X				
Interfaces	Receiver/DM/STATE			X		
Other (Linearity, Gain, Feedthrough, Crosstalk)	A/D Specifications		X			

Table A-III. Doppler Module Specifications

Speed	1.6 MHz Input Data Rate (I & Q)
Dynamic Range	11-bits Input/1-Bit Hard-limited Output
Memory Size	229K bits
Power Consumption	25 watts
Losses	1.8 dB
Program Instructions	Filter Weight Selection
BITE	Test Case
Reliability	7.24 f/10 ⁶ hours
Reconfiguration	3 out of 4 cold standby redundancy
Modularity	1 DM/board
Environmental	0°–120° F Operating; -70°–100° F Storage
Special Handling	Grounded Pins Carrier for CMOS Memory
Interfaces	A/D/Postfiltering Processor/STATE Processor

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For the complete SPUR, three parallel modules will be required to cover the Doppler spectrum, with a fourth channel added to provide redundancy. Since the modules are all identical except for the filter weights, we consider two channels sufficient to demonstrate all of the principle features, including fault detection and reconfiguration switching.

A.2.3 Postfiltering Processor

The Postfiltering Processor will consist of the biphase coded pulse compression unit and the envelope detector. Specifications for these functions are provided in Table A-V. During Phase II the following activities relating to the Postfiltering Processor will be conducted:

- a) Test a three-channel biphase coded pulse compression unit that is being developed in-house. Three channels are used to provide velocity offsets to reduce losses associated with high-velocity targets.
- b) Design, develop and test the envelope detection circuit.

The verification worksheet identifying the level of testing for the Postfiltering Processor is provided in Table A-VI.

Table A-IV. Verification Worksheet for Doppler Module (DM)

Characteristic	Requirement	Verification Approach				Remarks
		Analysis	Unit Level Demo	Processor Level Demo	System Level Demo	
Speed	1.6 MHz		X			Input Data Rate
Dynamic Range	11 Bits Input/Hard limited Output		X			Compatible with A/D
Memory Size	229 K bits	X			X	Words/Batch
Power	25 Watts		X			
Losses	1.8 dB	X			X	Near Optimum Filter
Program Instructions	Selection of Weights			X		
BITE/Calibration	Test Case			X		
Reliability	7.24 $\frac{1}{10^6}$ hr	X				MIL-HDBK-217B,C
Reconfiguration	3 of 4			X		Demo 1 of 2 Switching
Modularity	2 Units/Board		X			
Environmental	0° - 120° F Operating -70° - 100° F Storage	X				
Special Handling	Grounded Pins Carrier	X				
Interfaces	A/D/PFP/State			X		

Table A-V. Postfiltering Processor Specifications

Speed	1.82 MHz
Dynamic Range	1-bit Hard-limited Input; 6-bits Output
Power Consumption	16 watts
Losses	3.6 dB (including CFAR)
BITE	Test Case
Reliability	7.39×10^6 hours
Modularity	1 Board
Environmental	0°–120°F Operating; -70°–100°F Storage
Interfaces	Doppler Modules/Post Detection Processor/Zero Channel Processor/ STATE Processor

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Table A-VI. Verification Worksheet for Postfiltering Processor (PFP)

Characteristic	Requirement	Verification Approach				Remarks
		Analysis	Unit Level Demo	Processor Level Demo	System Level Demo	
Speed	1.82 MHz		X			In-House Equipment
Dynamic Range	Hard Limited Input 6-Bits Output		X			In-House Equipment
Memory Size	None					
Power	16 Watts	X	X			
Losses	3.6 dB	X		X	X	Including CFAR
Program Instructions	None					
BITE/Calibration	Test Case		X			
Reliability	7.39 $\times 10^6$ hr	X				MIL-HDBK-217B,C
Reconfiguration	None					
Modularity	1 Board		X			
Environmental	0° - 120° F Operating -70° - 100° F Storage	X				
Special Handling	None	X				
Interfaces	DM/PDP/ZCP/STATE			X		

A.2.4 Zero Channel Processor

The Zero Channel Processor and its associated memory are used to provide for detection of crossing, or zero-Doppler, targets. Preliminary specifications are given in Table A-VII. During Phase II the Zero Channel Processor will be partially demonstrated using a software program currently under in-house development. Changes to the program will provide the recommended map cell size. Memory for only a segment of the radar volume will be provided. The verification worksheet of Table A-VIII describes the validation procedures to be used for the Zero Channel Processor.

A.2.5 Postdetection Processor

The Postdetection Processor performs the *greatest of* channel selection and post detection integration operations. Specification for these units are provided in Table A-IX. During Phase II, we will design, develop and test the Postdetection Processor with validation procedures conducted as indicated on the verification worksheet of Table A-X.

A.2.6 STATE Processor Unit

The STATE Processor Unit is the controller for the SPUR. It monitors the BITE signals of the other processor units, directs interunit tests, reconfigures the processor when faults are indicated, and continually evaluates and reports the processor status. The STATE Processor Unit is a critical item in the SPUR, especially in terms of processor reliability and maintainability. We will design, develop, and test the STATE Processor Unit during the Phase II program. The STATE Processor will be integrated with the Doppler Filter Modules for demonstration of recovery from faults using redundant units.

Specifications for the STATE Processor Unit are listed in Table A-XI and the verification worksheet is given in Table A-XII.

Table A-VII. Zero Channel Processor Specification

Speed	3.6 μ sec/cell
Dynamic Range	6-bits in map
Clutter Map Memory Size	64K words/16K spare bank
Power Consumption	40 watts for RPM-II
Program Instructions	280
BITE	Test Cases
Reliability	9.11 f/10 ⁶ hours (1/2 interface board + RPM-II)
Reconfiguration	4/5 Memory Modules required 1/2 RPM-II's required
Modularity	1 Interface board, 2 RPMs
Environmental	0° - 120° F Operating; -70° - 100° F Storage
Interfaces	Post Filtering Processor/Post Detection Processor/ STATE Processor

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Table A-VIII. Verification Worksheet for Zero Channel Processor (ZCP)

Characteristic	Requirement	Verification Approach				Remarks
		Analysis	Unit Level Demo	Processor Level Demo	System Level Demo	
Speed	3.6 μ sec/cell		X			
Dynamic Range	6 Bits	X				
Memory Size	64K words	X			X	
Power	RPM-II 40W		X			
Losses	-	X			X	
Program Instructions	280 Instructions			X		
Stability/Calibration	Test Case			X		
Reliability	9.11 $f/10^6$ hr (RPM-II + $\frac{1}{2}$ Interface Bd)	X				
Reconfiguration	4/5 Memory Modules $\frac{1}{2}$ RPM-II	X				
Modularity	1 interface board 2 RPM-IIs		X			
Environmental	0° - 120° F Operating -70° - 100° F Storage	X				
Special Handling		X				
Interfaces	PFP/STATE/PDP			X		

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Table A-IX. Postdetection Processor Specifications

Speed	550 words/1.95 msec
Dynamic Range	6-bits Input/1-bit Output
Memory Size	4K bits
Power	35 Watts (Interface Board Only)
Losses	1.4 dB
Program Instructions	155 Instructions
BITE	Test Case
Reliability	7.9 f/10 ⁶ hours (½ Interface Board Only)
Reconfiguration	1 of 2 RPMs
Modularity	1 Interface board/2 RPM boards
Environmental	0° – 120° F Operating; -70° – 100° F Storage
Interfaces	Postfiltering Processor/Zero Channel Processor/STATE Processor

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Table A-X. Verification Worksheet for Posidetection Processor (PDP)

Characteristic	Requirement	Verification Approach				Remarks
		Analysis	Unit Level Demo	Processor Level Demo	System Level Demo	
Speed	550 words/1.95 msec		X			Input Data Rate
Dynamic Range	6-Bits Input		X			Multinomial Integrator
	1-Bit Output		X			
Memory Size	4K Bits	X			X	
Power	35 Watts Interface Board		X			
Losses	1.4 dB	X			X	
Program Instructions	155 Instructions			X		
BITE/Calibration	Test Case					
Reliability	7.9 f/10 ⁶ hr 1/2 Interface Board	X				
Reconfiguration	1 of 2 RPMs	X				
Modularity	1 Interface Board/2 RPM Boards		X			
Environmental	0° - 120° F Operating	X				
	-70° - 100° F Storage					
Special Handling	None	X				
Interfaces	PFP/STATE/ZCP			X		

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Table A-XI. State Processor Unit Specifications

Speed	5 MHz
Word Size	16 bits
Memory Size	16K Words Program Memory 2K Words Data Memory
Power	22 watts
Program Instructions	(TBD) Instructions
BITE	Internal Test Cases Processor Test Cases
Reliability	4.0 f/10 ⁶ hours
Reconfiguration	Triple Modular Redundancy
Modularity	1 Board
Environmental	0°–120° F Operating; -70°–100° F Storage
Interfaces	A/D Converter/Doppler Modules/Postfiltering Processor/ Zero Channel Processor/Post Detection Processor

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AD-A091 189 ITT GILFILLAN VAN NUYS CA F/6 17/9
SIGNAL PROCESSOR FOR UNATTENDED RADAR (SPUR) PHASE II.(U)
AUG 80 J M MILAN, C D LUCAS, D M KIKUTA F30602-78-C-0288
UNCLASSIFIED RADC-TR-80-254 NL

AD-A091 189 ITT GILFILLAN VAN NUYS CA F/6 17/9
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UNCLASSIFIED RADC-TR-80-254 NL

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Table A-XII. Verification Worksheet for State Processor

Characteristic	Requirement	Verification Approach				Remarks
		Analysis	Unit Level Demo	Processor Level Demo	System Level Demo	
Speed	5 MHz	X	X			
Dynamic Range	Word Size \geq 8 Bits		X			
Memory Size	16K Words Program Mem/ 2K Data Mem			X		
Power	22 Watts		X			
Losses	N/A					
Program Instructions	(TBD) Instructions			X		
BITE/Calibration	Test Cases					Internal Checks Processor Check
Reliability	4.0 $f/10^6$ hr	X				
Reconfiguration	Internal Redundancy		X	X	X	TMR
Modularity	1 Board		X			
Environmental	0° - 120° F Operating -70° - 100° F Storage	X				
Special Handling	None	X				
Interfaces	A/D/DM/PFP/ZCP/PDP				X	

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Appendix B

DOPLER FILTER MODULE UNIT DESIGN REQUIREMENT

A. PURPOSE OF THE UNIT

1. The Doppler Filter Module (DFM) shall be capable of performing the calculations required to implement two filters in a bank of narrowband filters. The filter bank shall consist of six PROM programmable Finite Impulse Response (FIR) filters. Each filter shall depend on eight complex data samples. The module shall provide storage, sufficient to process data for a maximum of 2048 range bins. Each module shall be capable of processing two filters.
2. In the SPUR system four DFM modules shall be provided, three will be powered up in an on-line mode and one shall be powered down in an off-line mode. All modules are identical. The off-line module filters can be substituted in place of any two of the 6 on-line filters. Control is by the STATE Processor.
3. In the SPUR test-bed two modules (four filters) shall be provided.

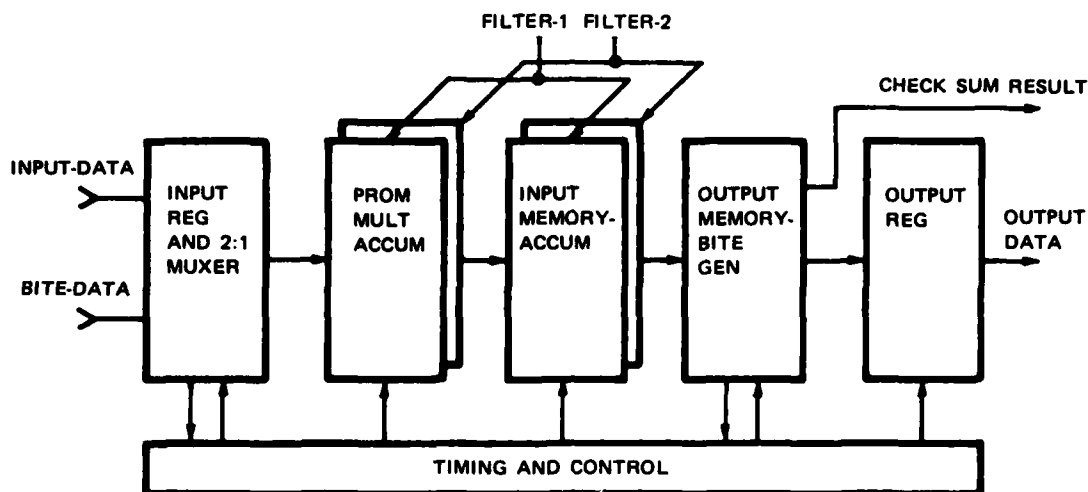
B. REQUIRED FUNCTIONAL CHARACTERISTICS (Figure B-1)

1. The DFM filter bank shall have the following characteristics:
 - a. Filter type; Finite Impulse (FIR) (See Section I).
 - b. Number of input data samples: 8 (complex)
 - c. Number of filters implemented: 6 (two per module).
2. The DFM shall provide an interface to the A/D Converter. The A/D Converter bus will have the following characteristics:
 - a. I channel data: 11 bits data + 1 - bit parity
 - b. Q channel data: 11 bits data + 1 - bit parity
 - c. Data rate: 618 nsec

Notes:

In the SPUR test bed the A/D interface shall be the following:

- a. I channel data: 10 bits
 - b. Q channel data: 10 bits
 - c. Data rate: 618 nsec
3. The module shall provide an interface to the State Processor. The State Processor shall be capable of doing the following functions:
 - a. Identify the Filter which the module is to process
 - b. Initiate built-in-test processing in the module
 - c. Receive the result of built-in-test processing
 - d. Switch the individual module and filters on line or off line. Designate the filters by assigning addresses to the PROM of the filters.
 - e. Provide the 24 bit BITE data.

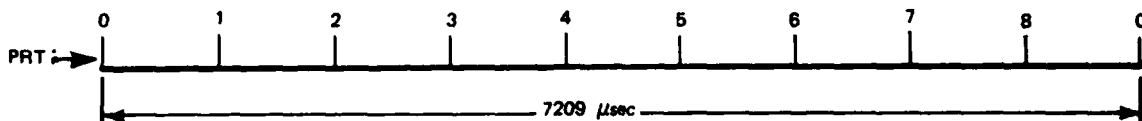


*Figure B-1. Functional block diagram of a DFM
(Two filters in the module)*

4. The DFM shall receive all clocks and synchronizing triggers from the Test Bed Interface Unit. The DFM shall receive the following clocks.
 - a. 618 nsec and
 - b. 309 nsec
5. The DFM shall provide hard limited data (sign bit only) to the Pulse Compressor. It shall also provide the following data to the State Processor.
 - a. Result of parity checks of the input data
 - b. Result of the output memory checksum test
6. The DFM shall provide filter output data for designated test range bins to the State Processor.
7. The input and output data timing sequences shall be as shown in Figures B-2 and B-3.

C. REQUIRED PHYSICAL CHARACTERISTICS

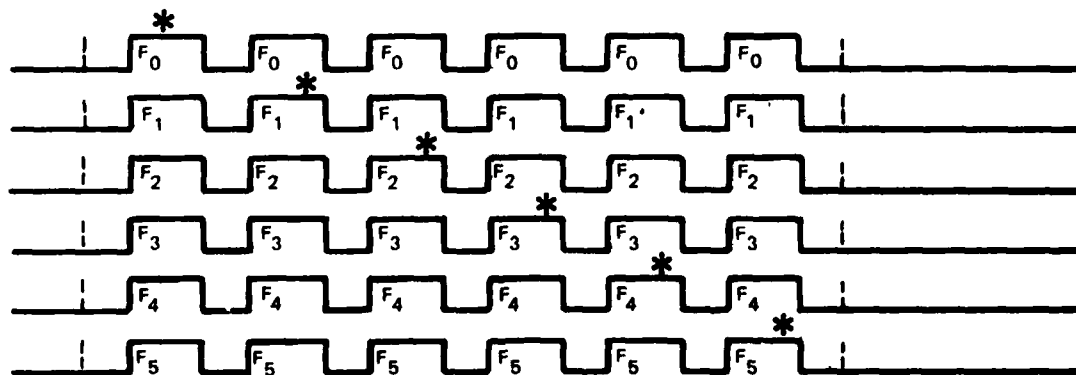
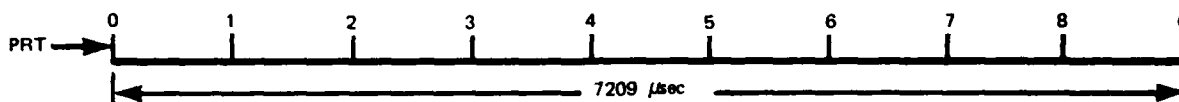
- a. The DFM shall be packaged on a single 14 by 15 inch wire-wrap board with an IC capacity of 210 sixteen pin packages. The board shall be fitted with the 2-1/2 tier connector.
- b. The wire-wrap board layout shall be easily convertible to a multiwire board layout based on the 210 sixteen pin package ITTG standard layout.
- c. The unit shall present a single 54LS298 load (or equivalent) on input data lines at the A/D interface.
- d. The unit shall operate on +5 VDC



NOTE: MINIMUM PRT SHOWN



Figure B-2. I/O data sequences of DFM



* NORMAL DATA OUTPUT POSITION

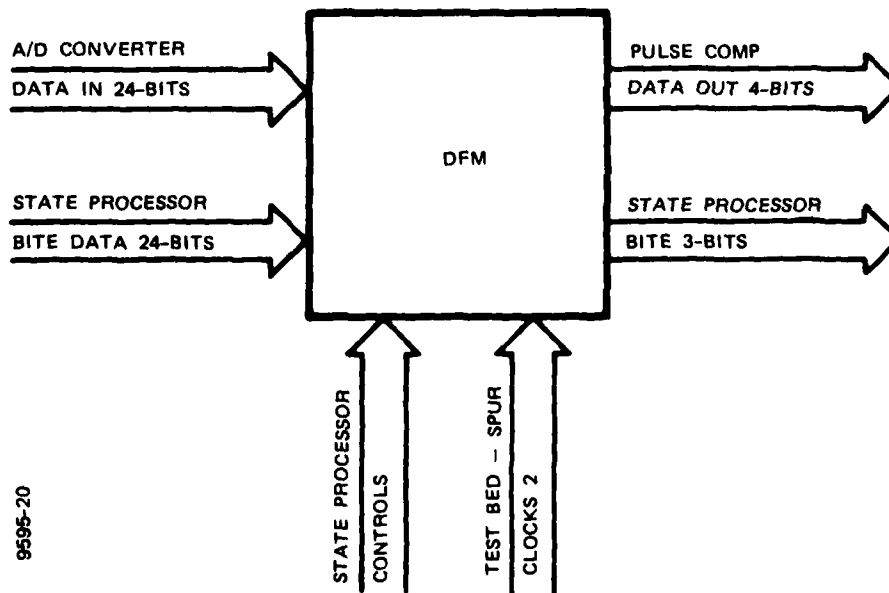
Figure B-3. Output from output memory

D. SPECIFICATION REQUIREMENTS

1. The unit shall meet the requirement of:
 - a. Post Filtering Processor
 - b. A/D Converter of the SPUR
 - c. State Processor
2. Environmental test requirements shall be as follows:
 - a. Operating temperature between 0°F to +120°F
 - b. Storage temperature between -70°F to +100°F

E. I/O SIGNAL REQUIREMENTS (Figure B-4)

<u>Bus</u>	<u>Signal</u>	<u>Comments</u>
DIB	24 bits	Data input bus
DOB	4 bits	Data output bus
CLK	2	Clocks
CONTROL	TBD	Range, Timing, Triggering
BITE	24 bits	Input data
	TBD	Output data and control



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Figure B-4. I/O configuration.

- F. COST GOALS: \$5,000.00/Board
- G. FAILURE RATE OF THE SYSTEM: 7.9745148/10⁶ hrs
- H. POWER DISSIPATION: 48.6 Watts
- I. FILTER EQUATIONS:

Let $X(n) = I+jQ$ = Input Data

$$A_{K,n} e^{j\theta_{K,n}} = P+jR = \text{weighting function}$$

The general equation of the filter is:

$$F(K) = \sum_{n=0}^{N-1} A_{K,n} X(n) e^{j\theta_{K,n}} \quad (1)$$

In the DFM, $N=8$, $K=0, \dots, 5$ and $n=0, \dots, 7$.

From equation (1)

$$F(0) = \text{Filter zero} = A_{0,0}X(0)e^{j\theta_{0,0}} + \dots + A_{0,7}X(7)e^{j\theta_{0,7}}$$

$$F(5) = \text{Filter five} = A_{5,0}X(0)e^{j\theta_{5,0}} + \dots + A_{5,7}X(7)e^{j\theta_{5,7}}$$

Now,

$$\begin{aligned} A_{K,n} X(n) e^{j\theta_{K,n}} &= (I+jQ) (P+jR) \\ &= (IP-QR) + j(PQ+IR) \end{aligned} \quad (2)$$

From equation (2), to calculate one filter, 32 real multiplications, and 16 real additions or subtractions are required.

J. WEIGHTS FOR RBDM FILTERS

<u>Filter Number</u>	<u>Center Frequency /PRF</u>	<u>Weight</u>	<u>Real</u>	<u>Imag</u>	<u>Amp</u>	<u>Phase</u>
0		W(0)	0.5441	0	0.5441	0
		W(1)	2.4091		2.4091	
		W(2)	5.4572		5.4572	
		W(3)	7.9453		7.9453	
		W(4)	7.9453		7.9453	
		W(5)	5.4572		5.4572	
		W(6)	2.4091		2.4091	
		W(7)	0.5441		0.5441	
1	0.30	W(0)	1.1318	0.0000	1.1318	0.0
		W(1)	-1.2983	-2.7667	3.0562	244.86
		W(2)	-4.2994	3.7345	5.6948	139.02
		W(3)	6.1737	4.2115	7.4734	34.30
		W(4)	2.4577	-7.0576	7.4734	289.20
		W(5)	-5.6775	-0.4447	5.6948	184.48
		W(6)	0.6021	2.9962	3.0562	78.64
		W(7)	0.9099	-0.6732	1.1318	323.50
2	0.39	W(0)	1.0257	0.0000	1.0257	0.00
		W(1)	-2.6701	-1.7004	3.1655	212.49
		W(2)	1.4243	5.5166	5.6975	75.52
		W(3)	3.2791	-6.6788	7.4403	296.15
		W(4)	-6.8814	2.8292	7.4403	157.85
		W(5)	5.4101	1.7867	5.6975	18.28
		W(6)	-1.5196	-2.7770	3.1655	241.31
		W(7)	-0.0680	1.0234	1.0257	93.80
3	0.50	W(0)	1.0000	0.0000	1.0000	0.00
		W(1)	-3.2680	0.0000	3.2680	180.00
		W(2)	5.6202	0.0000	5.6202	0.00
		W(3)	-7.4582	-0.0000	7.4582	180.00
		W(4)	7.4582	0.0000	7.4582	0.00
		W(5)	-5.6202	0.0000	5.6202	180.00
		W(6)	3.2680	-0.0000	3.2680	0.00
		W(7)	-1.0000	0.0000	1.0000	180.00
4	0.61	W(0)	1.0257	0.0000	1.0257	0.0
		W(1)	-2.6701	1.7004	3.1655	147.51
		W(2)	1.4243	-5.5166	5.6975	284.48
		W(3)	3.2791	6.6788	7.4403	63.85
		W(4)	-6.8814	-2.8292	7.4403	202.35
		W(5)	5.4101	-1.7867	5.6975	341.72
		W(6)	-1.5196	2.7770	3.1655	118.69
		W(7)	-0.0680	-1.0234	1.0257	266.20

<u>Filter Number</u>	<u>Center Frequency /PRF</u>	<u>Weight</u>	<u>Real</u>	<u>Imag</u>	<u>Amp</u>	<u>Phase</u>
		W(0)	1.1318	0.0000	1.1318	0.0
		W(1)	-1.2983	2.7667	3.0562	115.14
		W(2)	-4.2994	-3.7345	5.6948	220.98
		W(3)	6.1737	-4.2115	7.4734	325.70
5	0.70	W(4)	2.4577	7.0576	7.4734	70.80
		W(5)	-5.6775	0.4447	5.6948	175.52
		W(6)	0.6021	-2.9963	3.0562	281.36
		W(7)	0.9099	0.6732	1.1318	36.50

These weights shall be stored in a prom.

Appendix C

POST-FILTERING PROCESSOR

Section 1

SCOPE

This design note defines the Post-Filtering Processor. The functions to be added to the existing pulse compression board to modify and upgrade it to the Post-Filtering Processor are described.

1.1 INTRODUCTION

The Post-Filtering Processor (PFP) shall perform two major functions: three channel pulse compression and range combination. The three channel pulse compression function shall operate on complex (I and Q), hard-limited, 31 bit, binary-phase-coded data, using three effective channels to minimize losses due to Doppler sensitivity. The range combination function shall add odd and even range samples (i.e., $R_o = R_{2i} + 1 + R_{2i} + 2$, $0 \leq i \leq 554$) to reduce the double-sampled envelope-detected range data to a single value per range bin (0.1 nmi).

Binary-phase-codes are an attractive form of pulse compression, particularly from an implementation viewpoint, because they are relatively inexpensive and easy to build. However, a limiting drawback in the use of these codes is the Doppler sensitivity: substantial loss in signal-to-noise ratio (S/N) is incurred when targets have significant radial speed with respect to the radar (e.g., at L-band, a loss of 2.5 dB occurs on a 2400 knot target with a 31 bit code compressing to 1.25 μ sec). An ideal solution to this problem is to match the pulse compressor to the expected Doppler of the target; however, this solution requires estimation of the Doppler velocity and/or several pulse compression channels. An alternate solution to Doppler sensitivity is the three channel pulse compressor. It is an approximation to three channels, which allows some loss but has a much reduced hardware requirement.

Prior to the range combination function, two samples per range bin are processed from the A/D Converter through Doppler filtering and pulse compression. Two samples per range bin are used because range straddling losses are reduced by 1 dB when compared to single sampling. Positioning the range combination after pulse compression minimizes losses due to target position uncertainty (i.e., which samples should be combined; $R_i + R_i + 1$ or $R_i + 1 + R_i + 2$).

1.2 OTHER DOCUMENTS

Signal Processor for Unattended Radar (SPUR), Phase I, Final Report
28 March 1979

Section 2

FUNCTIONAL DESCRIPTION

The Post-Filtering Processor shall perform eight functions:

- 1) Preliminary Pulse Compression
- 2) Zero Channel Addition
- 3) Positive Doppler Channel Rotation
- 4) Negative Doppler Channel Rotation
- 5) Envelope Detections
- 6) Greatest-of Selection
- 7) Range Combination
- 8) BITE

The Preliminary Pulse Compression Function shall divide the 31-bit complex (time-multiplexed) input data in half and separately compress the resulting 15-bit and 16-bit sections using the similarly-divided 31-bit reference code. This compression shall be performed on the filtered hard-limited I and Q data from the Doppler Filter Modules or on BITE data located on the PFP.

The Zero Channel Addition Function shall combine the first half and second half results from the Preliminary Pulse Compression to form I and Q channels of compressed video. This function corresponds to the final stage of addition in a standard adder tree pulse compressor.

The Positive/Negative Doppler Channel Rotation Function shall combine the first half and second half results from the Preliminary Pulse Compression by first performing an approximation to a complex multiply on the second half of the data and then adding these results to the first half. I and Q channels of data are thereby formed.

The Envelope Detections Function shall perform an approximation to an envelope detection (rms summer) on the I and Q data from each of the three Doppler channels previously described.

The Greatest-of Selection Function shall compare the envelope-detected outputs from the three Doppler Channels and select the largest of these inputs as the output of this function. Therefore this function reduces the three channels back to a single channel for further processing.

The Range Combination Function shall add the odd and even successive data values to reduce the data rate to one sample per 0.1 nmi range bin.

The BITE Function shall provide the BITE data to the Preliminary Pulse Compression Function, detect the results of all three channels operating on this data, report errors to the STATE Processor, and accept extended BITE test commands from the STATE Processor.

The Preliminary Pulse Compression, Zero Channel Addition, one Envelope Detection, and portions of the BITE currently reside on a 14" X 15" standard multiwire board. The remaining functions will be implemented on a separate board interfaced to the existing board. A simplified Post-Filtering Processor Block Diagram is provided in Figure C-1.

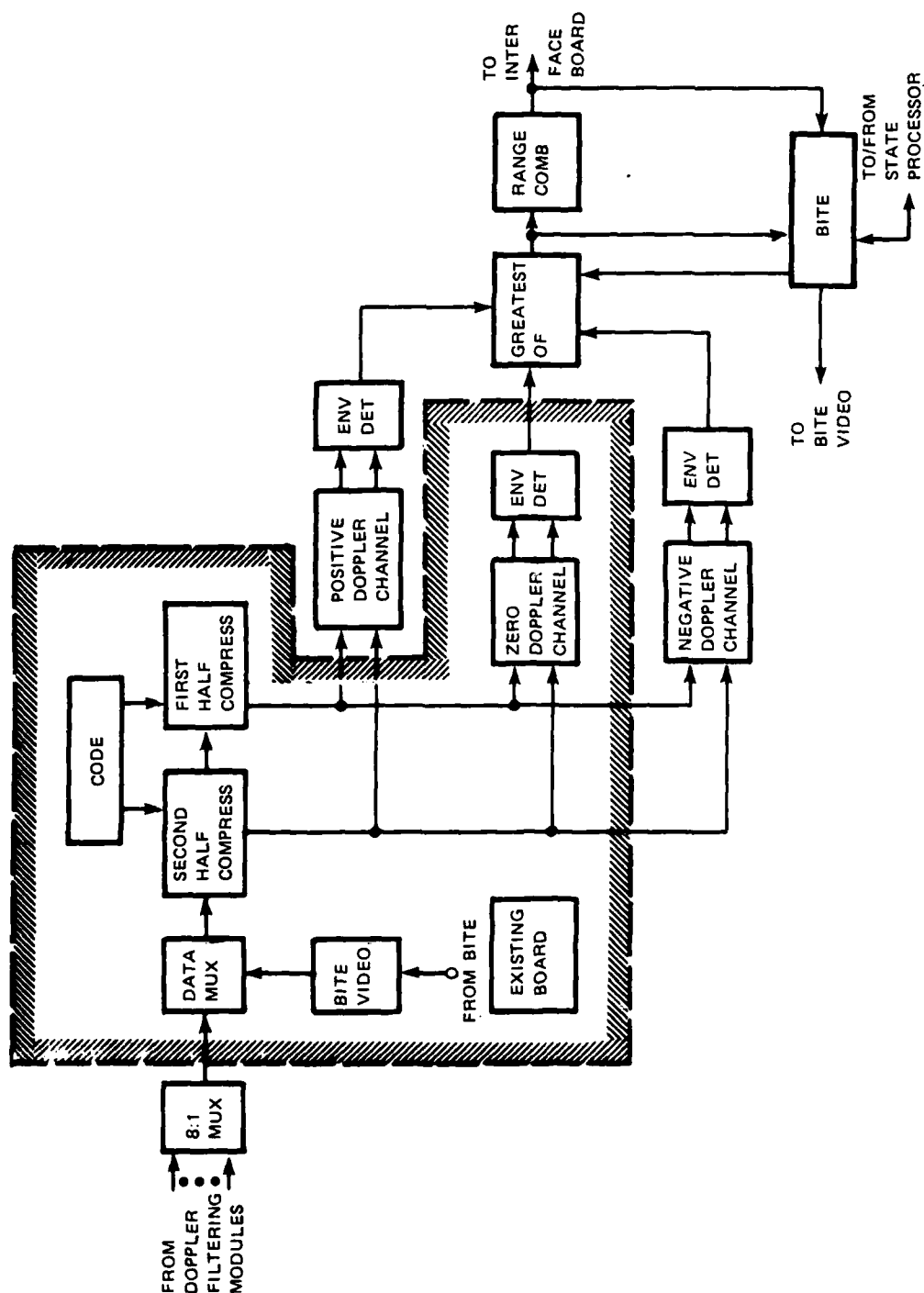


Figure C-1. Simplified functional block diagram

Section 3

UNIT DEFINITION

3.1 INTERFACES

The Post-Filtering Processor shall interface with the Doppler Filtering Modules, Interface Board, and STATE Processor of the SPUR. It shall also interface with the System Interface Board in the SPUR Phase II Test Bed for timing (clocks) and control signals. These interfaces are illustrated in Figure C-2.

3.2 SIGNAL PROCESSING FLOW DIAGRAM

Signal flow in the Post-Filtering Processor shall be as shown in Figure C-3 and discussed herein. Eight channels of hardlimited I and Q video shall be received from the Doppler Filtering Modules and selected by an 8:1 multiplexer as the input to the PFP. The multiplexer control shall be from the STATE Processor. The selected filtered video shall be presented to a 2:1 multiplexer. This multiplexer selects the input data or BITE data and time-multiplexes the I and Q channels for the subsequent pulse compression. The selected data is compared with the code in two sections (first 15 bits and last 16 bits) of exclusive OR gates and added in a four-level adder tree. This implementation, different than the recommended method for SPUR, uses existing hardware to reduce development costs. At the output of the four-level adder tree, the division into three channels is made.

The Zero Channel performs a fifth level of addition and aligns (demultiplexes) the I and Q data. The Envelope Detector performs the approximation to the rms summation:

$$V_o = \max (|I|, |Q|) + 1/4 \min (|I|, |Q|)$$

and sends the data to the Greatest-of Selection discussed below.

The positive and negative Doppler channels perform a phasor rotation (based on the worst case Doppler offset) of the second half of the pulse compressed data by using an approximation to a complex multiply:

$$I_2^1 + j Q_2^1 = (0.25 \pm j 1.0) (I_2 + j Q_2) = [0.25 I_2 \mp Q_2] + j[\pm I_2 + 0.25 Q_2]$$

The approximation is used to implement the multiply using only shifts and adds/subtracts. The rotated data is added to the first half data,

$$I + jQ = (I_1 + I_2^1) + j(Q_1 + Q_2^1)$$

to become the input data to two envelope detectors which are identical to the one previously described.

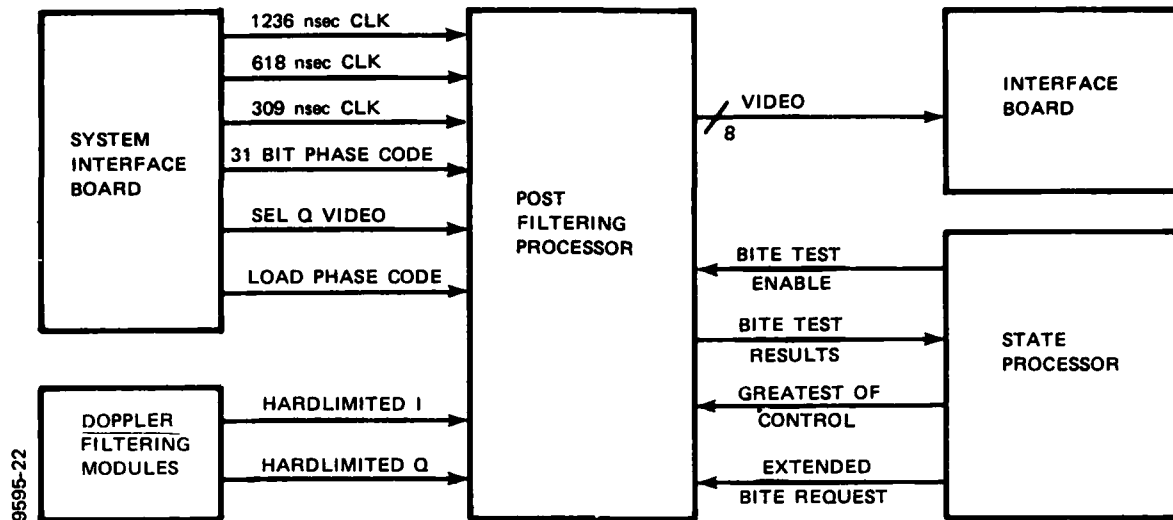


Figure C-2. Interfaces for post-filtering processor

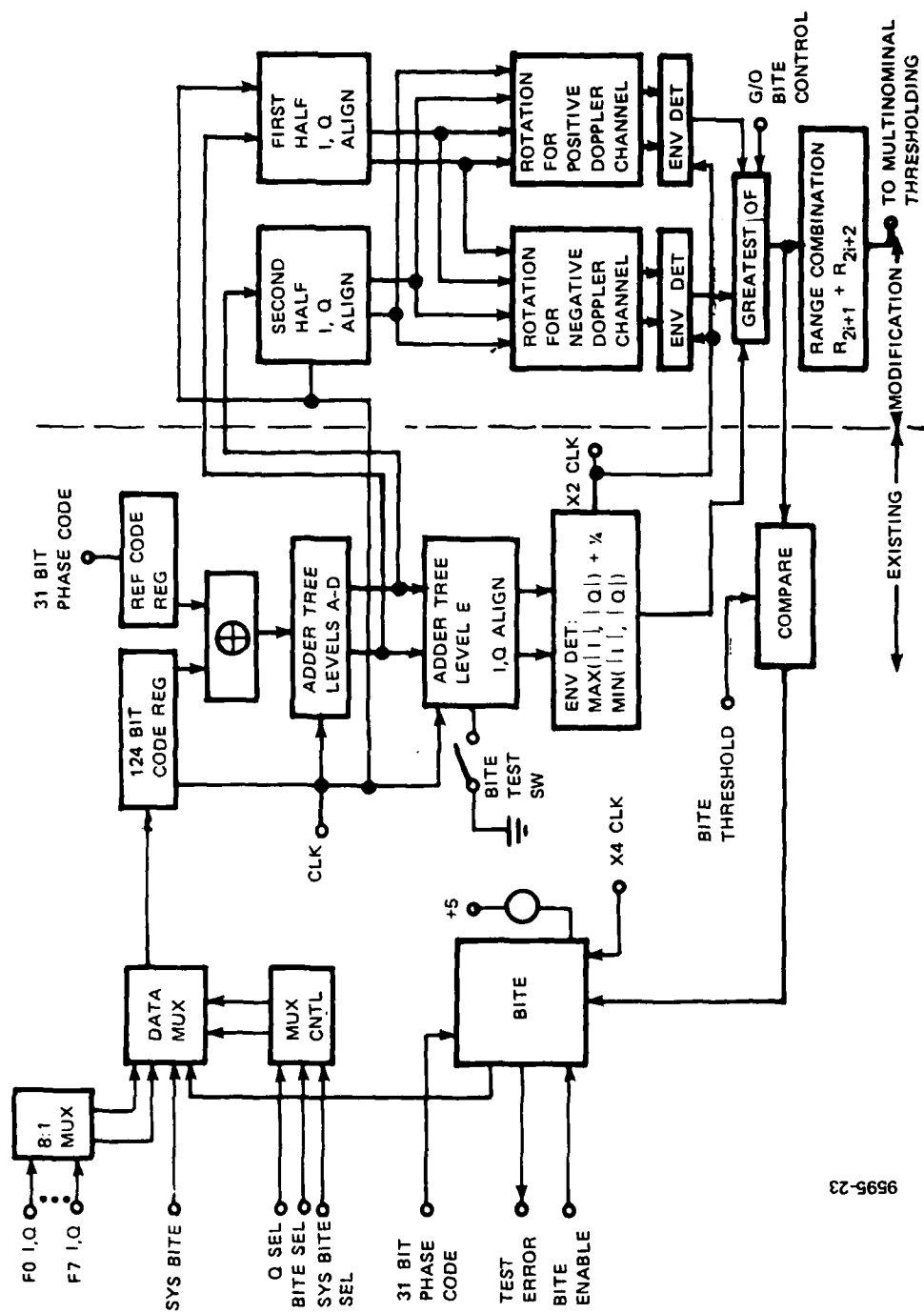


Figure C-3. Signal flow block diagram.

9595-23

The "greatest-of" selection compares the Data outputs from the three channels and selects the channel with the maximum amplitudes for further processing. Since all data is positive at this point, the selection process is straightforward.

The Range Combination adds the odd data samples to the even data samples to obtain one data sample per range bin (1.236 μ sec). Data is parity encoded at this point and sent to the Interface Board. This output data shall be eight bits including parity.

The BITE provides BITE video for test of the pulse compression channels, evaluates BITE signals at the output of the Range Combination, and controls the Greatest-of Selection should a failure occur in a single channel. The BITE, Interfacing with the STATE Processor, provides status outputs and receives control inputs.

3.3 TIMING

The Post-Filtering Processor shall receive three clocks for control of internal processing: the basic range bin rate clock of 1236 nsec and two submultiples of 618 nsec and 309 nsec. The Post Filtering Processor shall receive 1100 range samples of I and Q each at a 618 nsec rate during PRT times one through six. No data shall be received during PRT times zero, seven or eight. The Post Filtering Processor shall send output data at a rate of 1236 nsec during PRT times one through six for 550 range bins each. No data shall be sent during PRT times zero, seven, and eight. Data from the zero filter shall be received first and shall be sent first. Internally, the Preliminary Pulse Compression and Zero Channel Addition shall operate from the 309 nsec clock, the Positive/Negative Doppler Channel Rotation, the Envelope Detections and Greatest-of Selection shall use the 618 nsec clock, and the Range Combination Function shall operate at 1236 nsec. The BITE Function shall use each of the clocks as required at appropriate points in its operation. A simplified timing diagram is shown in Figure C-4.

3.4 PHYSICAL CHARACTERISTICS

The Post-Filtering Processor shall be fabricated using a 14 x 15 inch multiwire board containing a 31-bit single channel pulse compression function and an additional "piggyback" board containing the additions for the three channel operation.

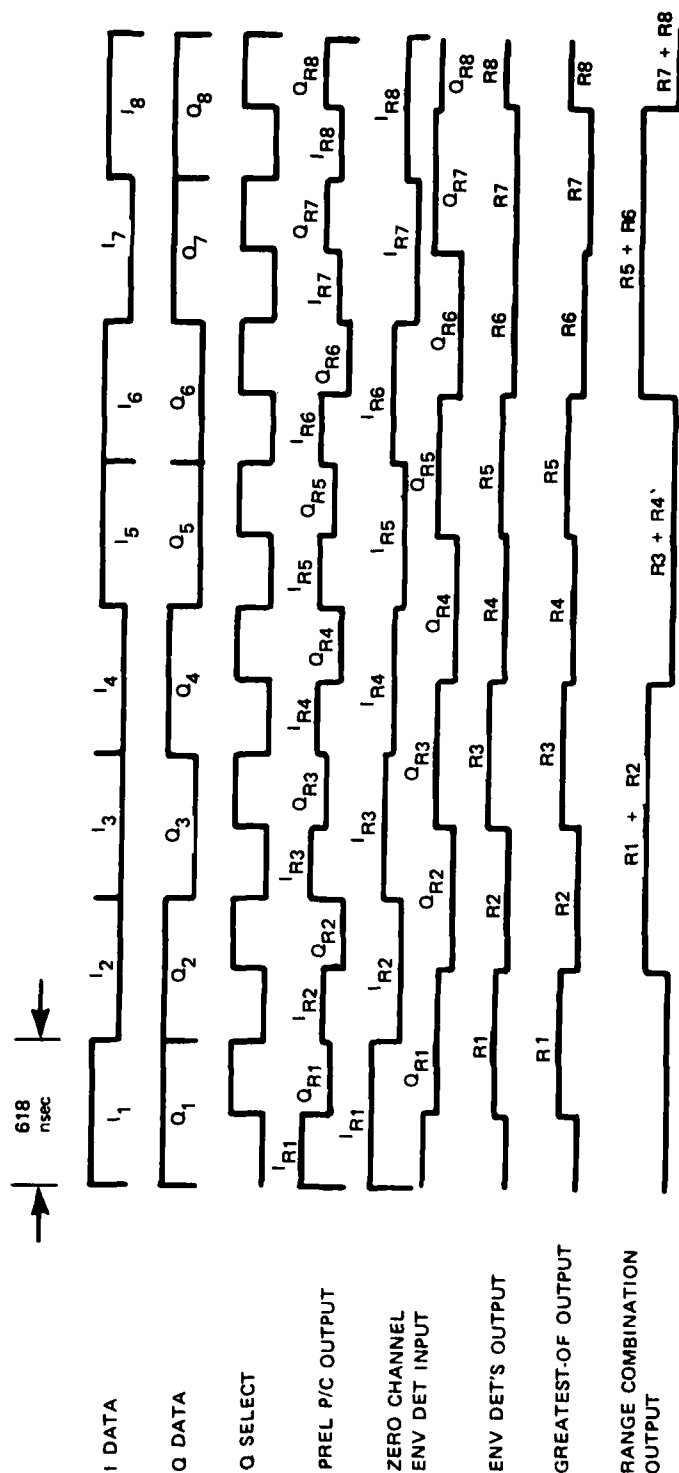


Figure C-4. Simplified timing diagram for Post-Filtering Processor

Appendix D

POST DETECTION INTEGRATION PROGRAM PROCESSING REQUIREMENT

1.0 SCOPE

1.1 IDENTIFICATION

This PPR establishes the performance requirements for the Postdetection Integration Computer program hereinafter referred to as the *PDI*. The *PDI* is part of the computer programs for the Signal Processing Project. This document, along with the design material (structured flowchart, database descriptions and program listing) and the Acceptance Test Plan, shall form the Final Technical Report.

1.2 FUNCTIONAL SUMMARY

This document details the functional (task) requirements of the *PDI*. The following is a list of the functions of this program:

- Initialization
- Input Routines
- Input Buffer Processing
- Cell History File Processing
- BITE Routines

A summary description of each of the above listed functions is contained in Section 3.1.2 and detailed descriptions are contained in Section 3.2.

2.0 APPLICABLE DOCUMENTS

Signal Processor for Unattended Radar (SPUR), Phase I, Final Report, 28 March 1979.

3.0 PROGRAM SPECIFICATIONS

3.1 PROGRAM DEFINITION

The Post-Detection Integration program performs a) noncoherent video integration of four two bit values (one azimuth beamwidth), and b) automatic target detection on the integrated video.

Noncoherent integration and automatic target detection for each of 550 range bins is performed using a multinomial detector in which detection is accomplished by a double threshold process. The first threshold, quantizing the digital video to two bits, is performed in hardware in the Interface Unit (by the Greatest-of-Filter, GOF) once each 9-pulse

transmission group. The PDI program formats the four, two bit words as an address for a PROM which performs the second threshold.

3.1.1 Interface Requirements

The PDI interfaces externally with the Interface Unit (IU) as shown in Figure D-1. All inputs to the PDI from the IU are listed in Table D-I. All outputs from the PDI to the IU are listed in Table D-II. All inputs and outputs are described in further detail in Section 4.0 referenced by the number in Tables D-I and D-II.

3.1.2 Primary Functions

3.1.2.1 Initialization

3.1.2.1.1 Description. This program function is run in response to a power-up interrupt condition. Program controls are set and the cell history file is cleared. At PRT seven, input and output FIFOs are cleared and processing begins.

3.1.2.1.2 Interfaces. The Initialization function interfaces with the IU for I/O and program control is passed to the BITE Routines.

3.1.2.2 Input Routines

3.1.2.2.1 Description. This program function stores all input Threshold Crossing Messages in an input buffer file and creates a table of azimuth from which final azimuth is calculated.

3.1.2.2.2 Interfaces. The Input Routines interface with the IU for external I/O and sends messages to the Input Buffer Processing function and the Cell History File Processing function. Program control is passed to the Input Buffer Processing function when the last cell for a transmission group has been input. BITE Routines are run while waiting for input messages.

3.1.2.3.1 Description. This program function stores Threshold Crossing Messages from the input buffer into the Cell History File. The Threshold Crossing Messages are broken into range and Threshold Crossing Code. The Threshold Crossing Codes are stored in the Cell History File, indexed by range, to form the Cell Bit pattern with three last previous Threshold Crossing Codes for that cell.

3.1.2.3.2 Interfaces. The Input Buffer Processing function receives messages from the Input Routines and sends messages to the Cell History File Processing function. Program control is passed to the Cell History File Processing function when all input words in the input buffer have been processed and stored in the Cell History File.

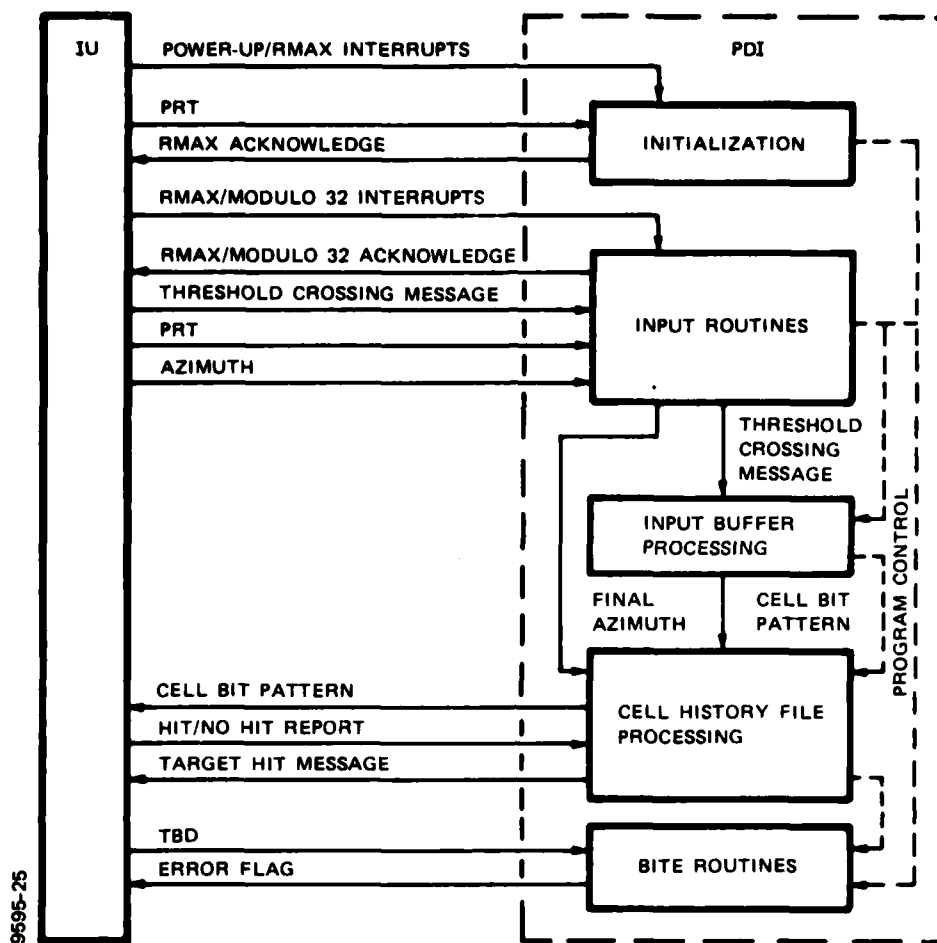


Figure D-1. External/internal interface

Table D-I. External Inputs

<u>Name</u>	<u>Reference No.*</u>	<u>Description</u>	<u>Source</u>	<u>Destination</u>
Azimuth	1	Requested Every RMAX Time, Used To Calculate Final Azimuth for Each Cell	IU	PDI
Hit/No Hit Report	4	Declares Target Hit or No Target Hit for Each Cell	IU	PDI
Modulo 32 Interrupt	5	Occurs When Input FIFO is Half Full	IU	PDI
Power-Up Interrupt		Occurs at Power Up Time	IU	PDI
PRT	6	Pulse Repetition Time	IU	PDI
RMAX Interrupt	5	Occurs Every RMAX Time	IU	PDI
Threshold Crossing	8	Codes Which GOF Detected Threshold is Crossed at a Range	IU	PDI

*Reference No. For Section 4.0.

Table D-II. External Outputs

<u>Name</u>	<u>Reference No.*</u>	<u>Description</u>	<u>Source</u>	<u>Destination</u>
Cell Bit Pattern	2	The Integrated Value of Four Threshold Crossing Codes, Used to Determine Hit or No Hit Status for Each Cell	PDI	IU
Modulo 32 Acknowledge		Acknowledges Modulo 32 Interrupt	PDI	IU
RMAX Acknowledge		Acknowledges RMAX Interrupt	PDI	IU
Target Hit Message	7	Sent for Every Range Cell With a Declared Target Hit	PDI	IU

*Reference No. For Section 4.0.

3.1.2.4 Cell History File Processing

3.1.2.4.1 Description. This program function sequentially cycles through the 550 word Cell History File. The contents of each location are sent out to a PROM multinomial threshold detector which declares whether the cell contains a target hit. For each cell with a declared target hit, a Target Hit Message is formatted and sent to the Data Processor for Unattended Radar (DPUR).

3.1.2.4.2 Interfaces. The Cell History File Processing function interfaces with the IU for external I/O. Internal inputs are received from the Input Routines and the Input Buffer Processing function. Program control is passed to the BITE Routines when the 550 word Cell History File has been completely cycled through and Target Hit Messages have been sent for all declared target hits.

3.1.2.5 BITE Routines

3.1.2.5.1 Description. This program function provides fault monitoring and isolation routines. This function schedules and executes RPM-II Diagnostic Routines (local standardized BITE) and the system test target. Other BITE will be used to exercise hardware specifically used by the PDI function to determine and check error conditions.

3.1.2.5.2 Interfaces. The BITE Routines interface with the IU through the BITE Serial Interface. Program control is passed on interrupt to the Input Routines.

3.2 DETAILED FUNCTIONAL REQUIREMENTS

3.2.1 Initialization

3.2.1.1 Inputs. Inputs to the Initialization function are the power-up interrupt, RMAX interrupt, and PRT. These inputs are listed in Table D-II and are further described and formatted in Section 4.0.

The power-up interrupt signals the start of the Initialization function. As RMAX interrupts occur, the PRT is read. At PRT seven, the input and output FIFOS are cleared and processing starts.

3.2.1.2 Processing. The Initialization performs the following processing.

- Set program controls (TBD).
- Clear Cell History File.
- Determine starting point for processing by clearing input and output FIFOS and passing program control at PRT 7.

3.2.1.3 Outputs. None

3.2.1.4 Special Requirements. None

3.2.2 Input Routines

3.2.2.1 Inputs. Inputs to the Input Routines are RMAX interrupt, Modulo 32 interrupt, Threshold Crossing Messages, PRT and Azimuth. These inputs are listed in Table D-II and further described and formatted in Section 4.0.

The Modulo 32 interrupt indicates a half full input FIFO and when received, the Input Routines unload the input FIFO into an input buffer. When RMAX interrupts occur the PRT is read, azimuth is read and stored in azimuth table. At PRT seven, the remaining words in the input FIFO are stored in an input buffer and a cell final azimuth is calculated from the azimuth table.

3.2.2.2 Processing. The Input Routines perform the following processing:

- Transfer of Threshold Crossing Messages from the input FIFO to an input buffer.
- Storage of azimuth in azimuth table.
- Calculation of final azimuth from azimuth table by taking an average value plus a pipeline delay factor.
- Check for last Threshold Crossing Message.

3.2.2.3 Outputs. Outputs from the Input Routines are the Final Azimuth and Threshold Crossing Messages. These outputs are listed in Table D-III and are further described and formatted in Section 4.0.

Table D-III. Internal Input/Output

<u>Name</u>	<u>Reference No.*</u>	<u>Description</u>	<u>Source</u>	<u>Destination</u>
Cell Bit Pattern	2	The integrated value of four threshold crossing codes, used to determine hit or no hit status for each cell.	Input Buffer Processing	Cell History File Processing
Final Azimuth	3	Azimuth associated with each cell.	Input Routines	Cell History File Processing
Threshold Crossing Message	8	Codes which GOF detected. Threshold is crossed at a range.	Input Routines	Input Buffer Processing

*Reference No. For Section 4.0.

The Final Azimuth is calculated from the azimuth table and is output to the Cell History File Processing function. The Threshold Crossing Messages are sent unchanged to the Input Buffer Processing function through an input buffer.

3.2.2.4 Special Requirements. None.

3.2.3 Input Buffer Processing

3.2.3.1 Inputs. Input to the Input Buffer Processing function are Threshold Crossing Messages. This input is listed in Table D-III and is further described and formatted in Section 4.0.

Threshold Crossing Messages are read from an input buffer and each Threshold Crossing Code is stored in the Cell History File to form the Cell Bit Pattern with the three last previous Threshold Crossing Code in that range.

3.2.3.2 Processing. The Input Buffer Processing performs the following processing:

- Read Threshold Crossing Messages from the input buffer.
- Mask out the Threshold Crossing Code and the range from the Threshold Crossing Message.
- Store Threshold Crossing Codes in the Cell History File indexed by range.

3.2.3.3 Outputs. Output from the Input Buffer Processing function is the Cell Bit Pattern. This output is listed in Table D-III and further described and formatted in Section 4.0.

The Cell Bit Pattern is stored in the Cell History File and is updated with each new Threshold Code.

3.2.3.4 Special Requirements. 560 word cleared memory required for Cell History File.

3.2.4 Cell History File Processing

3.2.4.1 Inputs. Inputs to the Cell History File Processing function are the Cell Bit Pattern, final azimuth and the Hit/No Hit Report. These inputs are listed in Tables D-I and D-III and are further described and formatted in Section 4.0.

The Cell Bit Pattern is sequentially read from the Cell History File and used as an address for PROM. The Hit/No Hit Report is input from PROM at the location addressed by the Cell Bit Pattern. The final azimuth was calculated previously and is used in formatting Target Hit Messages.

3.2.4.2 Processing. The Cell History File Processing performs the following processing:

- Sequentially, for the 550-word Cell History File, read Cell Bit Pattern and output as PROM address.
- For every declared target hit, format a Target Hit Message and output to Interface Unit.
- Shift each Cell Bit Pattern to provide room for the next Threshold Crossing Code and restore in Cell History File.

3.2.4.3 Outputs. Outputs to the Cell History File Processing function are the Cell Bit Pattern and the Target Hit Message. These outputs are listed in Table D-II and are further described in Section 4.0.

The Cell Bit Pattern is used as an address for the PROM containing the Hit/No Hit Reports. The Target Hit Message is outputted for every cell with a declared target hit.

3.2.4.4 Special Requirements. None.

3.2.5 BITE Routines

3.2.5.1 Inputs. Inputs to the BITE Routines will be as necessary to exercise all hardware functions and are TBD. An input test case to test firmware processing is also provided.

3.2.5.2 Processing. The BITE Routines perform the following processing:

- System test target.
- Specific test cases for the PDI function, to test PDI firmware and hardware specifically used during PDI. These will be in the form of regular BITE to determine error conditions and Extended BITE (EBITE) to check error conditions.
- RPM-II Diagnostic Routines (local standardized BITE).

3.2.5.3 Outputs. Output from the BITE Routines are error flags to indicate failures in hardware or firmware. The format of these error flags is TBD.

3.2.5.4 Special Requirements. None.

4.0 DETAILED MESSAGE INFORMATION

This section lists the contents of each input or output message

Name	— message name
Description/Purpose	— briefly identifies the use of the message
Source Function	— message origin
Destination Function	— message destination
Frequency Maximum Minimum	— maximum and minimum message frequency (per quadrant per second, per scan, etc.)
Parameter Name Subfields	— description name for each subfield in the message
Scaling	— indicates the number of bits in each subfield as follows: X,Y — X is the number of bits in the subfield Y is the number of bits to the right of the binary point.
Type	— describes the organization of the subfield information
logical	— the subfield may take on only two values, zero (false) or non-zero (true).
logical string	— each bit of the subfield is itself a logical variable.
integer	— a string of binary digits with the binary point assumed to be to the right of the last digit in the string. It may be "signed" or "unsigned".
fixed-point	— a string of binary digits with the binary point fixed as described under Scaling.
Range	— indicates the spread of values allowed in this subfield. Values are decimal unless otherwise noted.
Min	— the minimum value each subfield may take.

- | | |
|----------|--|
| Max | – the maximum value each subfield may take. |
| Units | – the units, if any, in which each subfield is measured. |
| Comments | – explanatory remarks. |
| Note | – N/A denotes not applicable in any of the above fields. |

Reference No. 1

Detailed Message Description

Name Azimuth _____

Description	Radar Azimuth

Source	Interface Unit	Frequency
--------	----------------	-----------

Destination	Input Routines	On Request Every Rmax Time
-------------	----------------	-------------------------------

Path	I/O Bus 2

Subfield Name	Scaling	Type	Range		Units	Comments
			Min.	Max.		
Azimuth	12.0	Integer	0.176	359.9	Degrees	

Message Format

A diagram of a 16-degree azimuth circle. The circle is divided into 16 equal segments, each labeled with a number from 0 to 15. The segment labeled 12 is highlighted with a red border. The word "Azimuth" is written in the center of the circle.

Reference No. 2

Detailed Message Description

Name Cell Bit Pattern

Description Video Integration of Four, Two Bit Logical Values

Source Input Buffer Processing

Frequency

Min: N/A

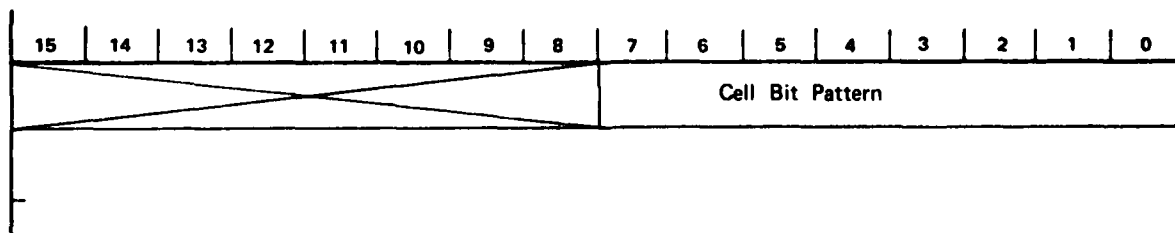
Max: N/A

Destination Interface Unit (via Cell History File Processing)

Path I/O Bus 1

Subfield Name	Scaling	Type	Range		Units	Comments
			Min.	Max.		
Cell Bit Pattern	8.0	Logical String	N/A	N/A	N/A	Sent for Each of the 550 Cells

Message Format



Reference No. 3

Detailed Message Description

Name	Final Azimuth
1	100
2	100
3	100
4	100
5	100
6	100
7	100
8	100
9	100
10	100
11	100
12	100
13	100
14	100
15	100
16	100
17	100
18	100
19	100
20	100
21	100
22	100
23	100
24	100
25	100
26	100
27	100
28	100
29	100
30	100
31	100
32	100
33	100
34	100
35	100
36	100
37	100
38	100
39	100
40	100
41	100
42	100
43	100
44	100
45	100
46	100
47	100
48	100
49	100
50	100
51	100
52	100
53	100
54	100
55	100
56	100
57	100
58	100
59	100
60	100
61	100
62	100
63	100
64	100
65	100
66	100
67	100
68	100
69	100
70	100
71	100
72	100
73	100
74	100
75	100
76	100
77	100
78	100
79	100
80	100
81	100
82	100
83	100
84	100
85	100
86	100
87	100
88	100
89	100
90	100
91	100
92	100
93	100
94	100
95	100
96	100
97	100
98	100
99	100
100	100

Description	Average Azimuth Value Plus Pipeline Delay
1.000000	1.000000
2.000000	2.000000
3.000000	3.000000
4.000000	4.000000
5.000000	5.000000
6.000000	6.000000
7.000000	7.000000
8.000000	8.000000
9.000000	9.000000
10.000000	10.000000
11.000000	11.000000
12.000000	12.000000
13.000000	13.000000
14.000000	14.000000
15.000000	15.000000
16.000000	16.000000
17.000000	17.000000
18.000000	18.000000
19.000000	19.000000
20.000000	20.000000
21.000000	21.000000
22.000000	22.000000
23.000000	23.000000
24.000000	24.000000
25.000000	25.000000
26.000000	26.000000
27.000000	27.000000
28.000000	28.000000
29.000000	29.000000
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38.000000	38.000000
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41.000000	41.000000
42.000000	42.000000
43.000000	43.000000
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77.000000	77.000000
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86.000000	86.000000
87.000000	87.000000
88.000000	88.000000
89.000000	89.000000
90.000000	90.000000
91.000000	91.000000
92.000000	92.000000
93.000000	93.000000
94.000000	94.000000
95.000000	95.000000
96.000000	96.000000
97.000000	97.000000
98.000000	98.000000
99.000000	99.000000
100.000000	100.000000


Source	Input Routines	Frequency
--------	----------------	-----------

Destination	Cell History File Processing	Calculated for Every Pulse Transmitted Group
1	2	3
4	5	6
7	8	9
10	11	12
13	14	15
16	17	18
19	20	21
22	23	24
25	26	27
28	29	30
31	32	33
34	35	36
37	38	39
40	41	42
43	44	45
46	47	48
49	50	51
52	53	54
55	56	57
58	59	60
61	62	63
64	65	66
67	68	69
70	71	72
73	74	75
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364	365	366

Path	Internal Register
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Subfield Name	Scaling	Type	Range		Units	Comments
			Min.	Max.		
Final Azimuth	12.0	Integer	0.176	359.9	Degrees	

Message Format

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				Final Azimuth											

Reference No. 4

Detailed Message Description

Name Hit/No Hit Report

Description Codes Whether Final Threshold has Been Crossed

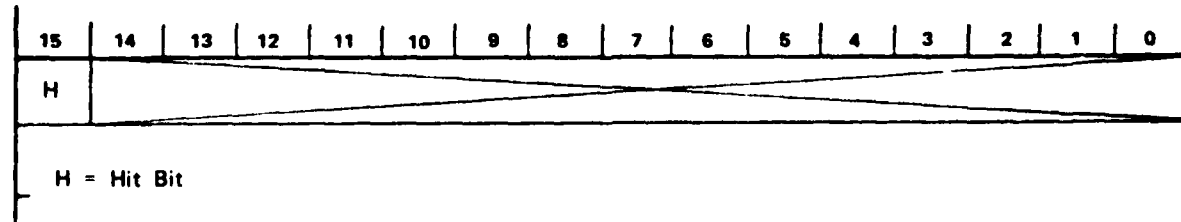
Source Interface Unit Frequency

Destination Cell History File Processing Input for Every Cell
Bit Pattern Output

Path I/O Port 1

Subfield Name	Scaling	Type	Range		Units	Comments
			Min.	Max.		
Hit Bit	1.0	Logical	0	1	N/A	1 = Hit 0 = No Hit

Message Format



Reference No. 5

Detailed Message Description

Name Modulo 32 and Rmax Interrupts

Description Modulo 32: Occurs When Input FIFO is Half Full
Rmax: Occurs Every Rmax Time

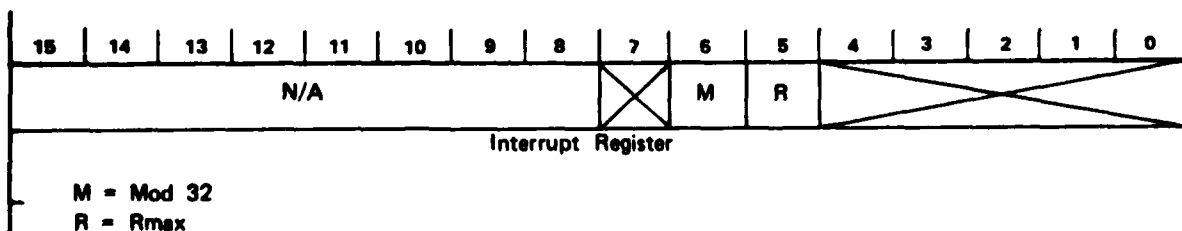
Source Interface Unit Frequency Rmax - Every Rmax Time

Destination Input Routines

Path Interrupt Lines

Subfield Name	Scaling	Type	Range		Units	Comments
			Min.	Max.		
Mod 32	1.0	Logical	0	1	N/A	1 = Interrupt 0 = No Interrupt
Rmax	1.0	Logical	0	1	N/A	1 = Interrupt 0 = No Interrupt

Message Format



Reference No. 6

Detailed Message Description

Name PRT

Description Number of Pulse in Transmission Group

Source Interface Unit Frequency

Destination Initialization, Input Routines On Request Every Rmax Time

Path I/O Bus 2

Subfield Name	Scaling	Type	Range		Units	Comments
			Min.	Max.		
PRT	4.0	Integer	0	9	N/A	

Message Format

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
												PRT			

Reference No. 7**Detailed Message Description**Name Target Hit MessageDescription Sent for Every Declared Target HitSource Cell History File Processing

Frequency

Destination Interface UnitFor Every Cell with
Target HitPath Output FIFO

Subfield Name	Scaling	Type	Range		Units	Comments
			Min.	Max.		
ID Code	2.0	Logical String	0	2	N/A	Identifies One of Three Words
Azimuth	12.0	Integer	0.176	359.9	Degrees	Final Azimuth Calculated for Each Cell
Range	10.0	Integer	0	550	nmi	
Cell Bit Pattern	8.0	Logical String	N/A	N/A	N/A	Cell Bit Pattern for Cell with Declared Target Hit

Message Format

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID Code															
ID Code															
ID Code															

Reference No. 8

Detailed Message Description

Name Threshold Crossing MessageDescription Occurs for Every Cell Containing a Crossing from the First ThresholdingSource Interface Unit Frequency
Average 6.2 for
Each Pulse TransmissionDestination Input Buffer Processing (via Input Routines)Path Input FIFO

Subfield Name	Scaling	Type	Range		Units	Comments
			Min.	Max.		
ID Code	3.0	Logical String	N/A	N/A	N/A	Identifies Message, One Fixed Code
Threshold Crossing Code	2.0	Logical String	1	3	N/A	Codes Which Threshold was Crossed
Last Cell Bit	1.0	Logical	0	1	N/A	1 = Last Cell 0 = Not Last Cell for Pulse Group
Range	10.0	Integer	0	55	nmi	

Message Format

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID Code			TCC		L	Range									
TCC = Threshold Crossing Code L = Last Cell Bit															

Appendix E

STATE PROCESSOR DESIGN NOTE

1.0 SCOPE

This design note provides initial definition of the Status, Transformation, and Test Evaluation (STATE) Processor. The STATE Processor is the central focus for reliability monitoring, control, and reporting in the Signal Processor for Unattended Radar (SPUR).

1.1 INTRODUCTION

The SPUR is a high performance, digital signal processor for a 2D, medium range, gap-filler type of radar. Because of its unattended nature, high reliability (with no loss of performance) is a major goal of the SPUR. The recommended SPUR uses fault-recovery techniques based on distributed BITE, selective redundancies, and centralized control (STATE Processor) to attain the performance/reliability goal.

BITE operations are distributed in the SPUR to allow automatic fault detection and isolation. BITE results for each unit are stored in a bidirectional BITE interface module located on each unit. The STATE Processor queries the BITE modules periodically and evaluates the BITE data. Upon discovery of a fault, the STATE Processor utilizes the selective redundancies of the SPUR to effect a repair. The goal of automatic fault discovery, isolation and recovery is on the order of one second.

The use of distributed BITE, selective redundancies, and the STATE Processor allows the SPUR to be fault-tolerant, thereby providing a major increase in MTBF for the SPUR over conventional radar signal processors.

1.2 OTHER DOCUMENTS

Signal Processor for Unattended Radar (SPUR), Phase I, Final Report, 28 March 1979

Reliability Prediction of Electronic Equipment, MIL-Hdbk-217C, 9 April 1979

2.0 FUNCTIONAL DESCRIPTION

The STATE Processor shall perform eight functions:

- Initialization and Self-Check
- BITE Data Evaluation
- Extended BITE Evaluation
- Reconfiguration
- SPUR Status Communication
- BITE and Redundancy Evaluation

- Degraded Modes Configuration
- Orderly SPUR Shutdown

The Initialization and Self-Check Function shall perform initial checks upon turn-on to verify that the STATE Processor is capable of proper operation. These checks shall include power-on reset in hardware, simple program to check STATE Processor sanity, memory I/O check, and BITE variables check.

The BITE Data Evaluation Function shall compare BITE data received from each module with stored BITE variables to detect malfunctions or verify proper operation of the modules.

The Extended BITE Evaluation Function shall compare Extended BITE data (EBITE) received from modules with a suspected failure with stored EBITE to verify failures and initiate recovery operations.

The Reconfiguration Function shall control recovery from module faults by deactivating failed modules, activating spare modules, and updating SPUR status. When no spares are available, this function shall call the Degraded Modes Function (described below).

The SPUR Status Communication Function shall maintain the status of all of the modules of the SPUR and shall periodically provide outputs of the status to the system. The SPUR Status Communication shall activate the orderly SPUR Shutdown Function when the status indicates a failed processor.

The BITE and Redundancy Evaluation Function shall periodically check the BITE and spares for proper operation. This function ensures that errors will be detected when they occur and that failed spares will not be activated.

The Degraded Modes Configuration Function shall initiate degraded modes operation if possible when normal operation cannot be maintained because of failures beyond the capacity of the SPUR selective redundancies. When degraded modes do not exist for the particular malfunction, the SPUR Status Communication Function shall be so notified.

The Orderly Processor Shutdown Function shall control shutting down the SPUR such that invalid data is not transmitted to the system. The shutdown shall include deactivation of failed modules where possible and maintaining storage of valid data where possible.

3.0 UNIT DEFINITION

3.1 INTERFACES

The STATE Processor shall interface with the other units of the SPUR; namely,

- A/D Converter Unit (ADCU)
- Doppler Filter Modules (DFM)
- Post Filtering Processor (PFP)
- Interface Board (IB)
- Radar Processing Module (RPM-II)

The data exchange between SPUR modules and the STATE Processor shall be serial. The STATE Processor shall have control on BITE data transfers through enable lines. The expected data transfers between units are listed in Table E-1.

Note: In the SPUR Test Bed, the STATE Processor shall interface only with the DFM for reliability control, monitoring, and demonstration at present.

In addition to the above SPUR interfaces, the STATE Processor shall interface with the following units of the SPUR Test Bed:

- Power Control Unit (PCU)
- System Timing Unit (STU)
- System Display Unit (SDU)

The interface to the PCU shall be for control of power to the active and spare DFM's and RPM-II's. The STU interface shall consist of clock inputs to the STATE Processor. The STATE Processor hardware shall monitor the clock for operation and provide an output upon loss of clock. The SDU interface shall allow display of SPUR status.

Note: In the SPUR Test Bed, this display shall consist of DFM and STATE Processor status at present.

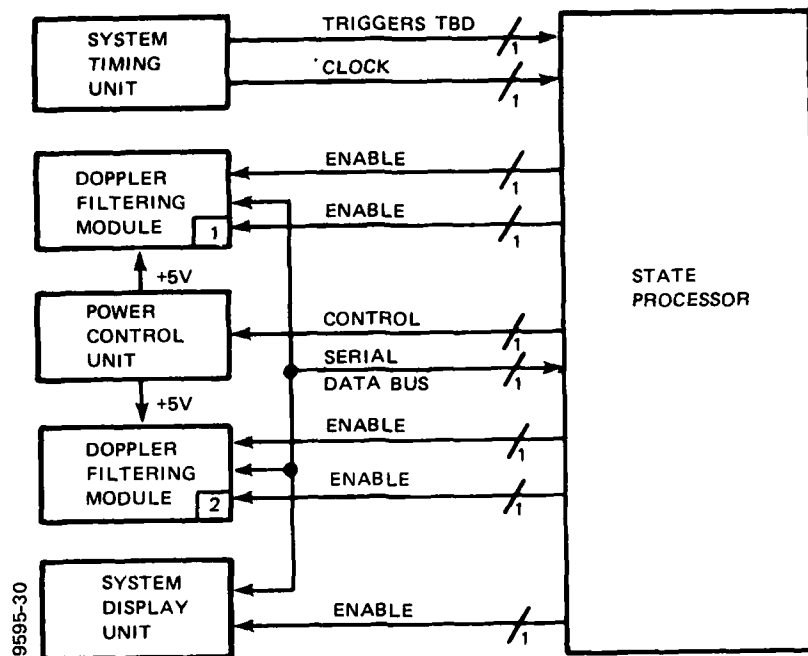
The SPUR Test Bed/STATE Processor Interface Block Diagram is shown as Figure E-1.

3.2 STATE PROCESSOR FLOW DIAGRAM

The STATE Processor Flow Diagram among functions is shown in Figure E-2. The Initialization and Self Check (ISC) Function shall be started by a power-on reset or external reset command. This function shall verify that the STATE Processor is capable of operating in a sane manner. Should a failure be detected, the SPUR Status Communication (SSC) Function shall be notified to provide a NO GO status to the system and the Orderly SPUR Shut-down (OSS) Function shall be called. Since faults which prevent communication to the system are possible, the system shall use a watchdog timer on the STATE Processor outputs; it shall cause an external reset after the first timeout and it shall force an Orderly SPUR Shutdown after the second consecutive timeout.

Table E-1. Data Transfer Between State Processor and Other Spur Modules

<u>Module</u>	<u>To State Data Processor</u>	<u>From State Processor</u>
A/D Converter	Active Channels Status of Standby Channel	BITE Read Enable Test Target Request BITE Test and Reset BITE Write Enable
Doppler Filter	BITE Results I Filter Data (16 Bits) Q Filter Data (16 Bits) Extended BITE Results I Filter Data (16 Bits) Q Filter Data (16 Bits) Parity Results on Input Data Checksum Results on Output Data	Filter Number Assignment and Extended BITE BITE Data (24 Bits) BITE Read Enable BITE Write Enable
Post Filtering Processor	BITE Results Channels Status	Filter Select Control BITE Read Enable BITE Write Enable
Interface Board	Detection of Double Error in Clutter Map Status of Clutter Map Modules BITE Results Clutter Map Interface Logic PDI Interface Logic	Memory Modules Active Control BITE Read Enable BITE Write Enable Degraded Modes Control Zero Channel Disable
Radar Processing Module (RPM-II)	BITE Results Processor Routine I/O Checks Extended BITE Results	RPM-II Selection Extended BITE Requests BITE Read Enable BITE Write Enable



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Figure E-1. Spur test bed/state processor interface

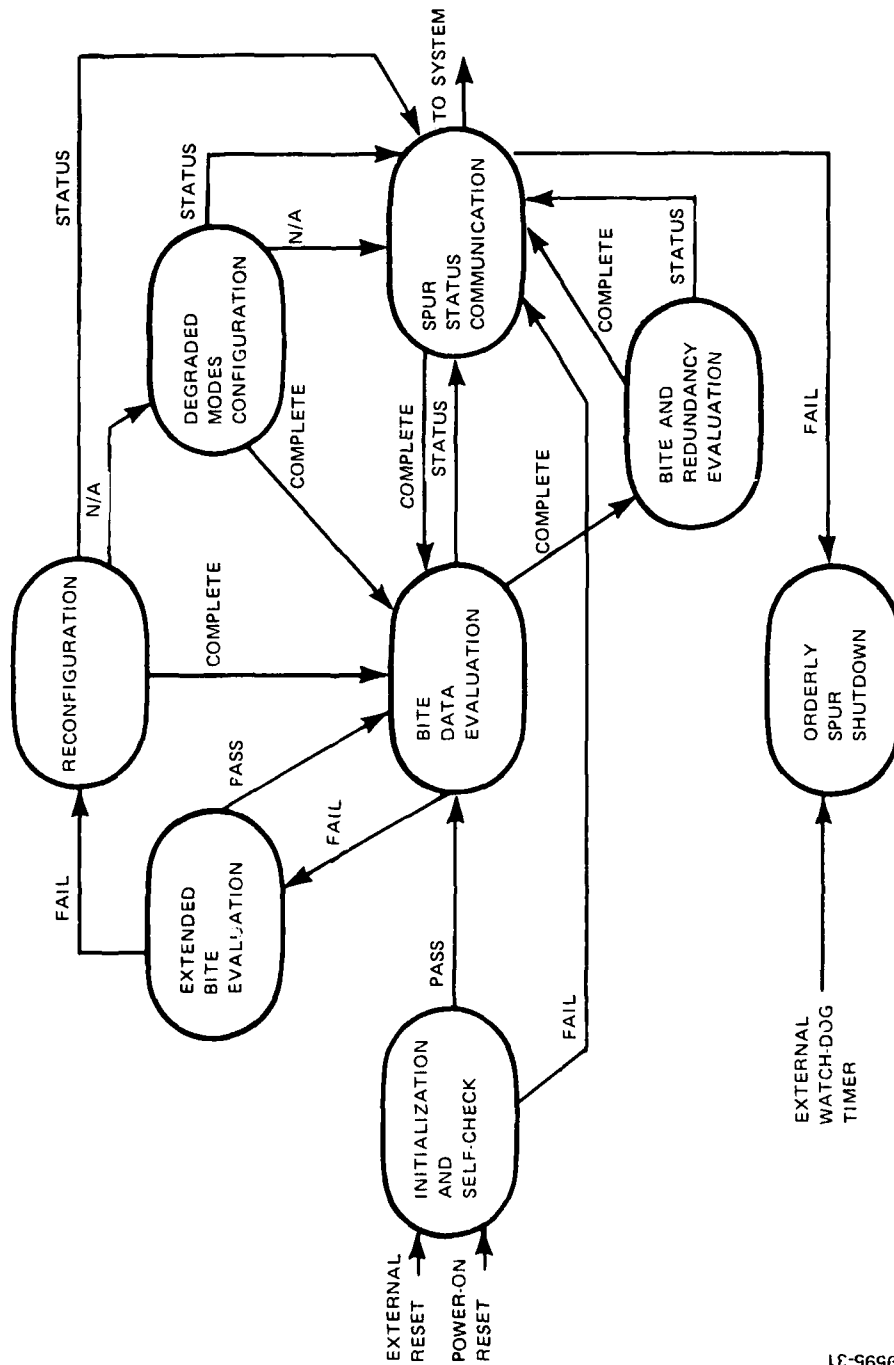


Figure E-2. State processor flow diagram

After initialization and self-check are complete, the ISC Function shall configure the system (i.e., turn-on the initially defined Doppler Filter Modules and RPM-II) and SPUR operations shall begin. Control shall be passed to the BITE Data Evaluation (BDE) Function.

The BDE Function shall provide BITE signals as required (see Interfaces, Section 3.1), interrogate each module to receive BITE results, and evaluate BITE results. When BITE data is correct, the next module in the sequence shall be interrogated. After all modules have been queried and no faults detected, the SPUR status shall be updated and the BITE and Redundancy Evaluation Function shall be called. However, if the BITE test for a module is failed, the Extended BITE Evaluation (EBE) Function shall be called.

The EBE Function shall request extended BITE (EBITE) for the questionable module and evaluate the results. When a failure is indicated, the Reconfiguration Function shall be called. However, when a failure is not indicated by the EBITE upon the first discovery of a fault by the BITE, control shall be returned to the BDE Function for retest because a transient is suspected. On a second failure of the same BITE, the Reconfiguration Function shall be called.

The Reconfiguration Function shall attempt to cause SPUR recovery by using selective redundancies. Should the fault be indicated in an area where selective redundancies do not exist, the Degraded Modes Configuration Function shall be called. Where selective redundancies exist, the Reconfiguration Function shall deactivate the failed module, activate the spare replacement module, and send configuration commands to this newly activated module. The SPUR status shall be updated to the SSC Function and control shall be returned to the BDE Function.

The SPUR Status Communication (SSC) Function shall communicate the status of all SPUR Modules to the system and shall decide, based on this status, whether the Orderly SPUR Shutdown Function shall be called. The communications to the system shall be within a specified time interval (TBD) such that the system watchdog timer is reset. The SCC Function shall normally be called by the BITE and Redundancy Evaluation (BRE) Function after status is checked. When communication is complete, control is returned to the BDE Function. Special cases occur when the ISC Function detects a failure or the Degraded Modes Configuration (DMC) has been called and no degraded modes exist for the failed condition. These two calls shall cause status communication to the system and a call to the Orderly SPUR Shutdown Function.

The Degraded Modes Configuration (DMC) Function shall activate degraded modes (which have been previously defined) when normal operation of the SPUR is not possible. A typical degraded mode is excising the zero filter when the clutter map is inoperative. The DMC Function shall provide status to the SSC Function and return control to the BDE Function. However, when no degraded modes exist for the identified failure, the DMC Function shall call the SSC Function.

The BITE and Redundancy Evaluation (BRE) Function shall provide BITE data to check the module BITE and selective redundancies. A typical method for performing these tests is to provide BITE data which causes the BITE to register an error. This error leads to reconfiguration to the spare module. Then this module is evaluated with the normal BITE and reset to the spare. Status is provided to the SSC Function and control is passed there also when the function is complete.

The Orderly SPUR Shutdown (OSS) Function shall shut down the failed SPUR such that invalid data is not transmitted to the system. This function is called by the SSC Function after the status of the SPUR is evaluated and transmitted to the system. The OSS Function can also be actuated by the system when the watchdog timer has timed out two consecutive times.

3.3 SPECIAL CHARACTERISTICS

The STATE Processor shall monitor the input clock and provide an output flag through hardware upon failure. When TMR is used to improve the reliability of the STATE processor, a disagreement detector in hardware with an output to the system shall be provided. BITE interfaces between the STATE Processor and SPUR modules shall be self-checking.

3.4 PHYSICAL CHARACTERISTICS

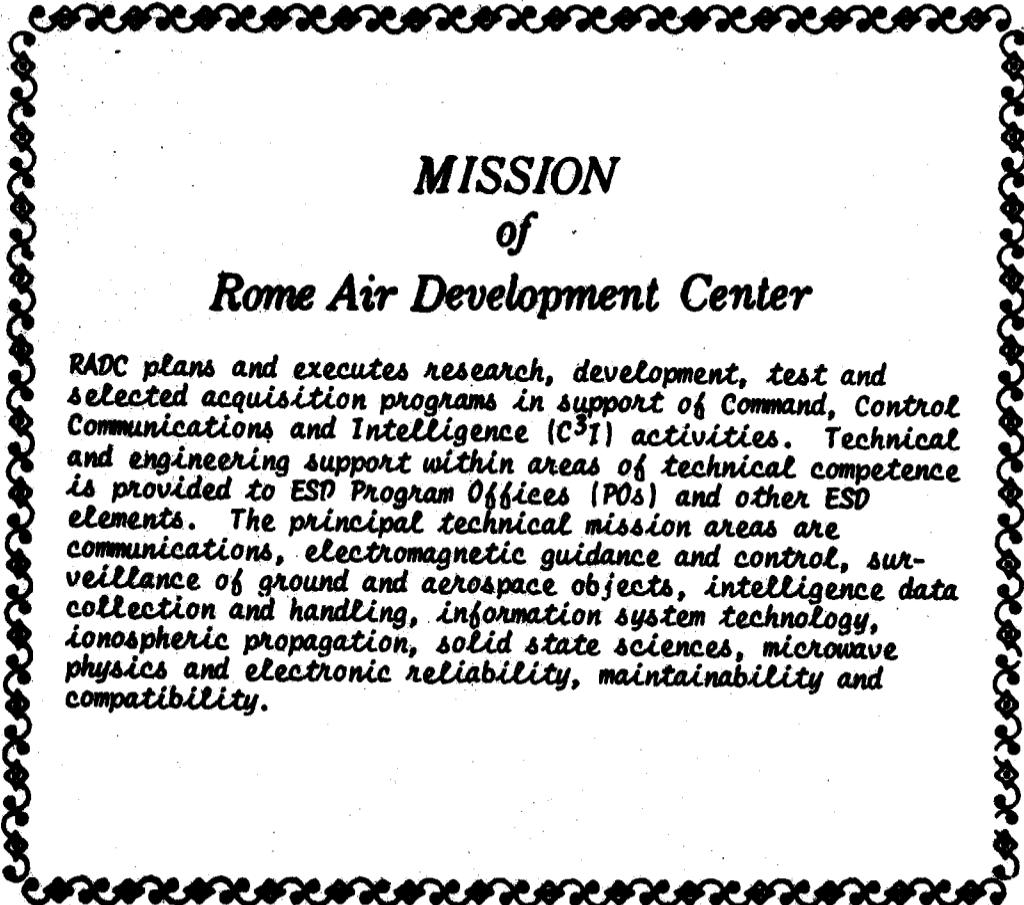
The STATE Processor shall be fabricated using a 14 X 15 inch wirewrap board containing a maximum of 210 16-pin equivalent chips. The firmware shall reside in PROMs.

3.5 GOALS

Since the STATE Processor is the central focus for reliability, it must be a highly reliable unit. Internal active redundancies (such as Triple Modular Redundancy (TMR)) shall be used so that the failure rate of the STATE Processor will be less than 25 percent of a typical board failure rate without redundancies. The goal is 4.0 failures per million hours. The calculation of failure rate shall be as described by MIL-Hdbk-217C with the following assumptions:

Learning Factor	$(\pi_L) = 1.0$	(Mature Devices)
Quality Factor	$(\pi_Q) = 2.0$	(Class B)
Environment Factor	$(\pi_E) = 1.0$	(Fixed Ground)
Temperature	$= 60^\circ\text{C}$	

The power dissipation goal is 25 watts.



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